

VER : 3A
PWA:W021J
PWB:W018J

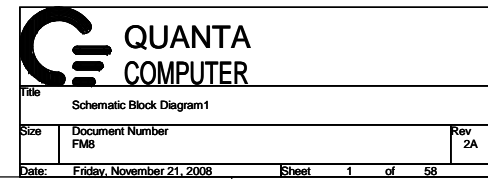








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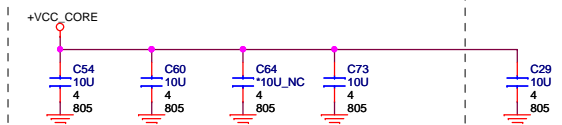
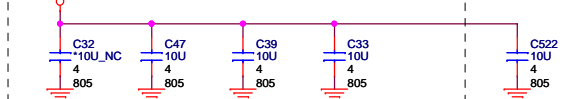
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| 45 | Blank Page |
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| 54 | DCin & Batt |
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| 58 | Power Block Diagram |

Power States

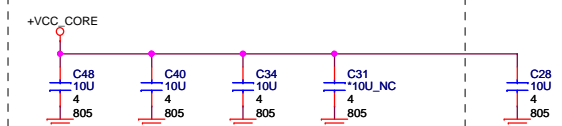
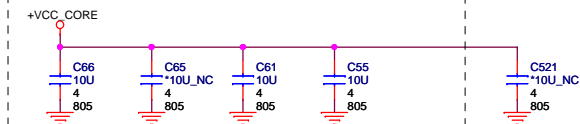
| POWER PLANE | VOLTAGE | PAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|----------------|--------------|---|--------------------------|-----------------------|-----------|
| +PWR_SRC | 10V~+19V | 4,26,32,34,46,48,49,50,51,52 | MAIN POWER | | S0~S5 |
| +RTC_CELL | +3.0V~+3.3V | 11,14,31,32 | RTC | | S0~S5 |
| +3.3V_ALW | +3.3V | 3,13,31,32,36,37,38,44,46,49,52,53,54 | 8051 POWER | ALWON | S0~S5 |
| +5V_ALW2 | +5V | 38,48,49,52,53,54 | LARGE POWER | RUN_ON | S0~S5 |
| +3.3V_LAN | +3.3V | 42,43 | LAN POWER | AUX_ON | |
| +5V_SUS | +5V | 14,35,36,38,50,51,52,53 | SLP_S5# CTRLD POWER | SUS_ON | |
| +3.3V_SUS | +3.3V | 3,11,12,13,14,20,26,30,38,43,48,50,51,53 | SLP_S5# CTRLD POWER | SUS_ON | |
| +1.8V_SUS | +1.8V | 6,8,9,15,48,49,50,53 | SODIMM POWER | SUS_ON | |
| +0.9V_DDR_VTT | +0.9V | 16,49,53 | SODIMM POWER | RUN_ON | |
| +5V_RUN | +5V | 14,20,26,27,36,37,39,40,41,53 | SLP_S3# CTRLD POWER | RUN_ON | |
| +3.3V_RUN | +3.3V | 3,6,8,9,11,12,13,14,15,17,20,22,26,27,28,30,31,33,34,36,39,40,41,42,51,53 | SLP_S3# CTRLD POWER | RUN_ON | |
| +1.8V_RUN | +1.8V | 19,20,21,22,23,38,53 | SDVO POWER | RUN_ON | |
| +1.5V_RUN | +1.5V | 4,9,14,30,31,33,34,48,53 | CALISTOGA/ICH9 POWER | RUN_ON | |
| +1.2V_LOM | +1.25V | 42 | LOM POWER | +3.3V_LAN | |
| +1.1V_GFX_PCIE | +1.1V | 21,50 | VGA POWER | RUN_ON | |
| +1.05V_VCCP | +1.05V | 3,4,5,6,8,9,11,14,48 | CPU/CALISTOGA/ICH8 POWER | 1.05V_RUN_ON | |
| +VCC_CORE | +0.7V~+1.77V | 4,51 | CPU CORE POWER | IMVP_VR_ON | |
| +LCDVCC | +3.3V | 26 | LCD Power | LCDVCC_TST_EN & ENVDD | |
| +5V_MOD | +5V | 36 | Module Power | MODC_EN | |
| +5V_HDD | +5V | 36 | HDD Power | HDDC_EN | |
| | | | | | |
| | | | | | |

| GND PLANE | PAGE | DESCRIPTION |
|--|------|-------------|
|  GND_CHG | 46 | |
|  GND_1.05V | 47 | |
|  GND_VGA | 50 | |
|  GND_SIGNAL | 51 | |
|  AGND_DC/DC | 52 | |
|  GND | ALL | |
| | | |

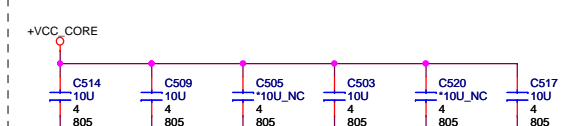
+VCC_CORE All use 10U 4V(+/-20%,X6S,0805)Pb-Free.



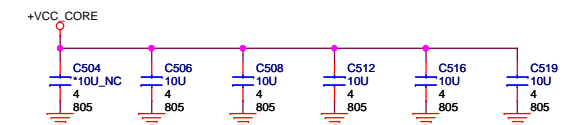
8 inside cavity, north side, secondary layer.



8 inside cavity, south side, secondary layer.



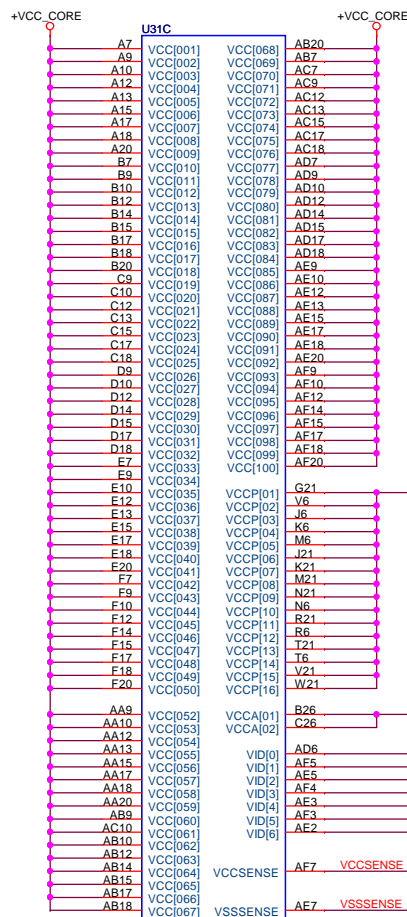
6 inside cavity, north side, primary layer.



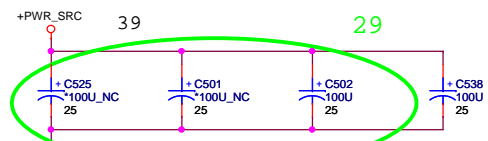
6 inside cavity, south side, primary layer.



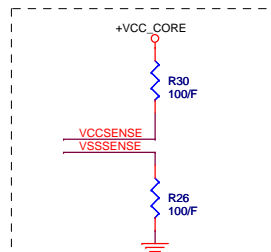
Layout out:
Place these inside socket cavity on North side secondary.



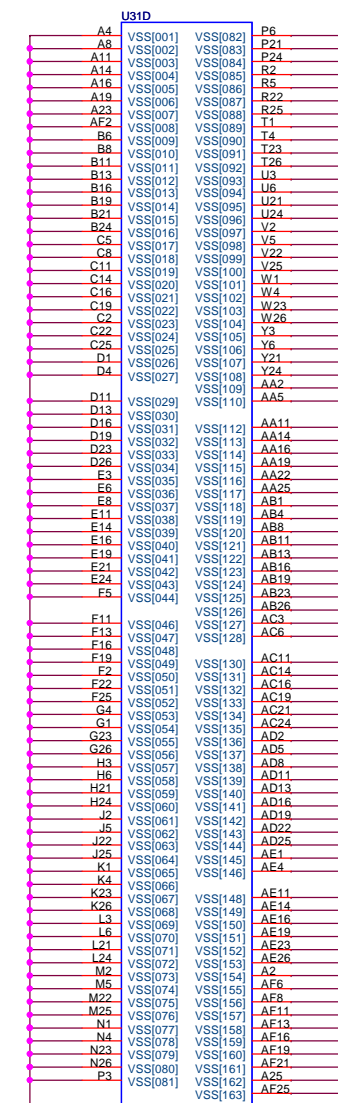
Penryn Ball-out Rev 1a



Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.

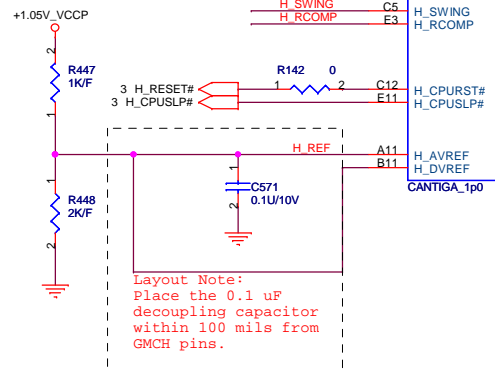
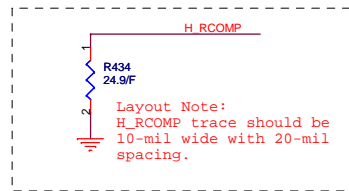
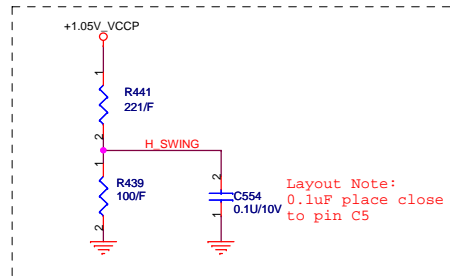


Route VCCSENSE and VSSSENSE
traces at 27.4ohms and
length matched to within 25
mil. Place PU and PD within
2 inch of CPU.

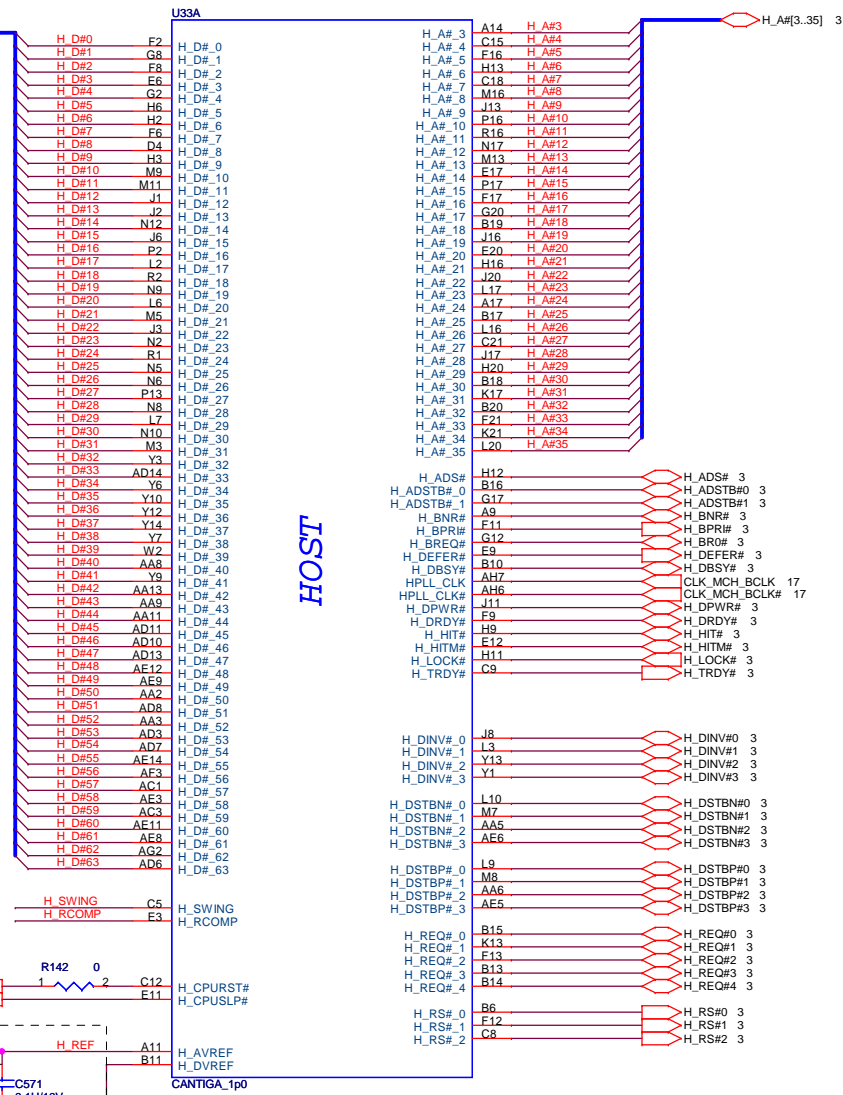


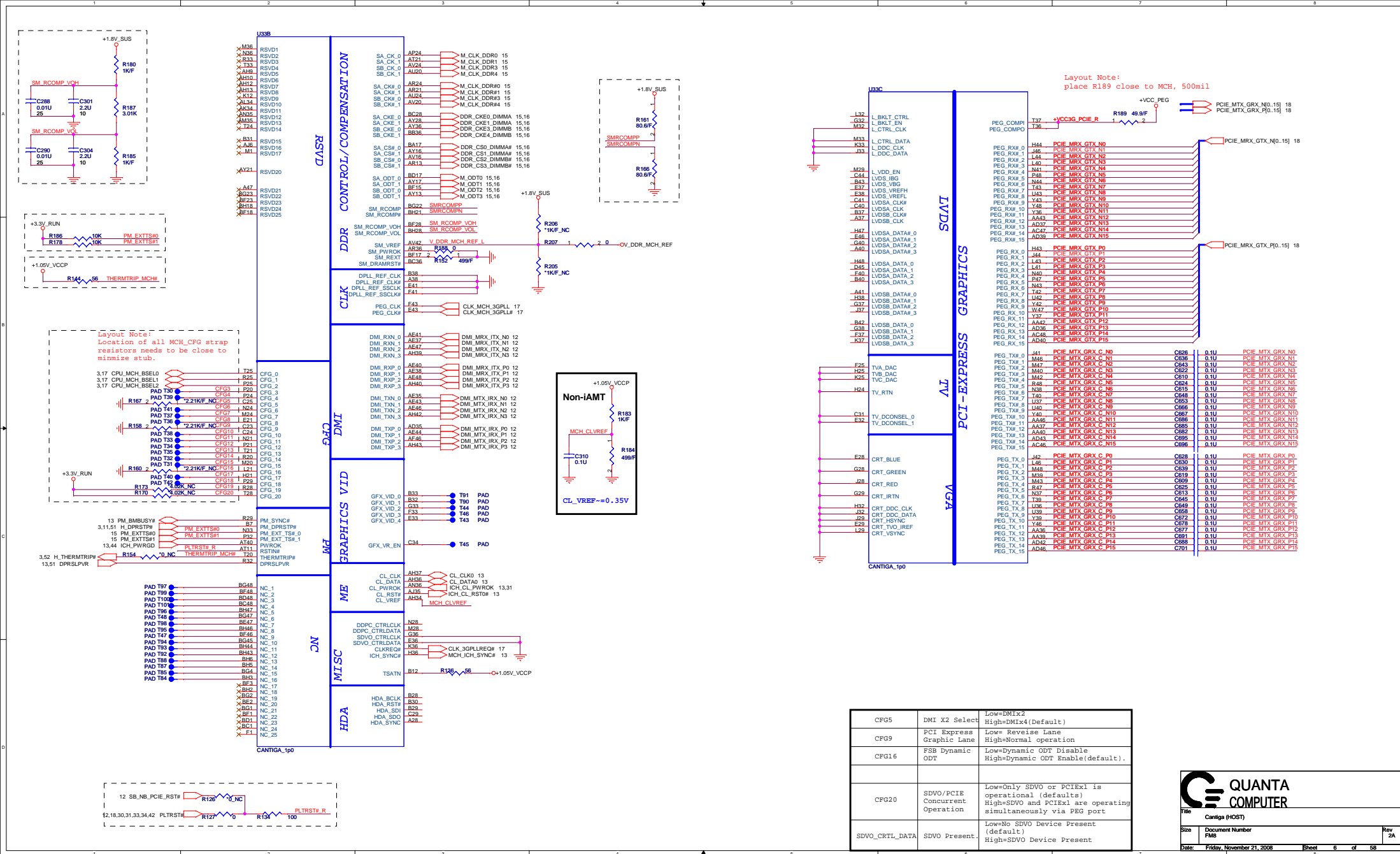
Penryn Ball-out Rev 1a

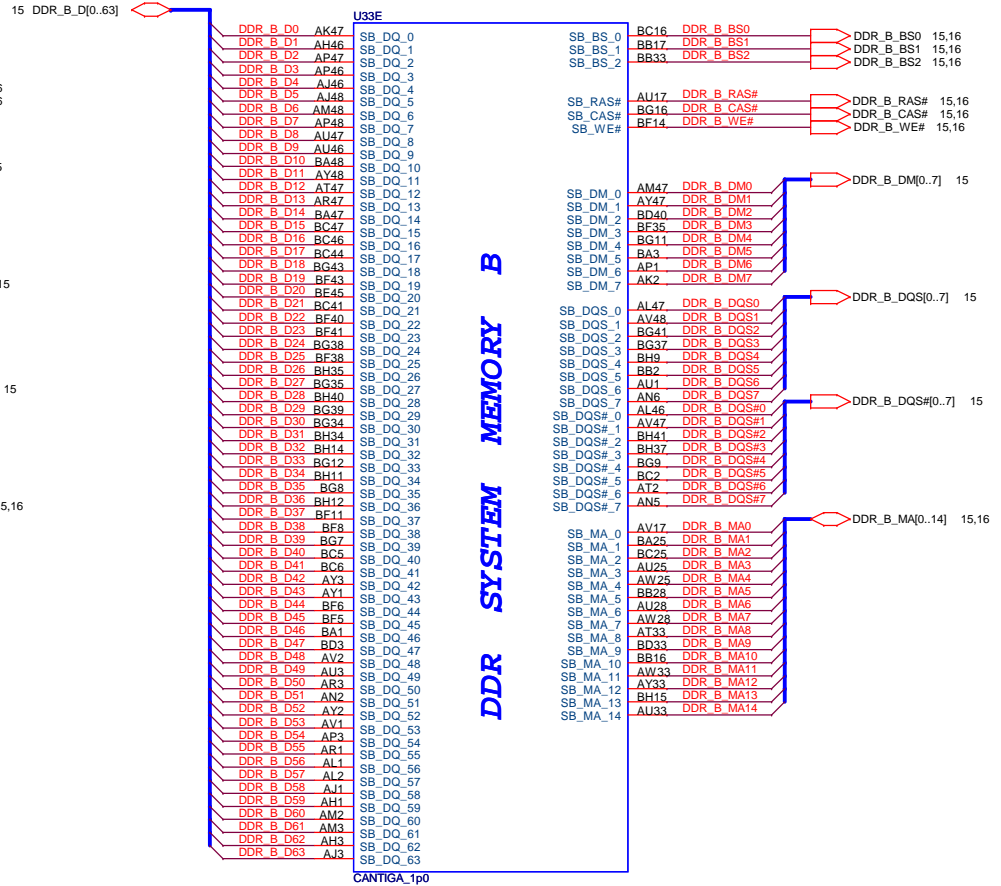
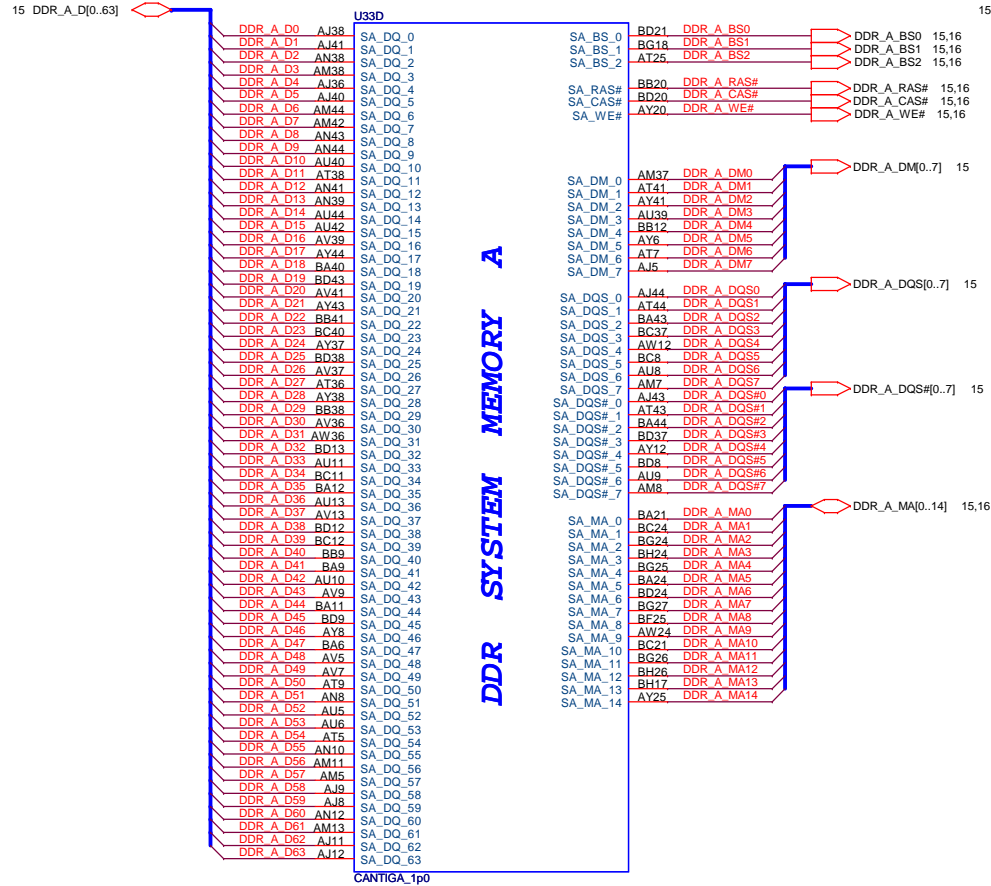


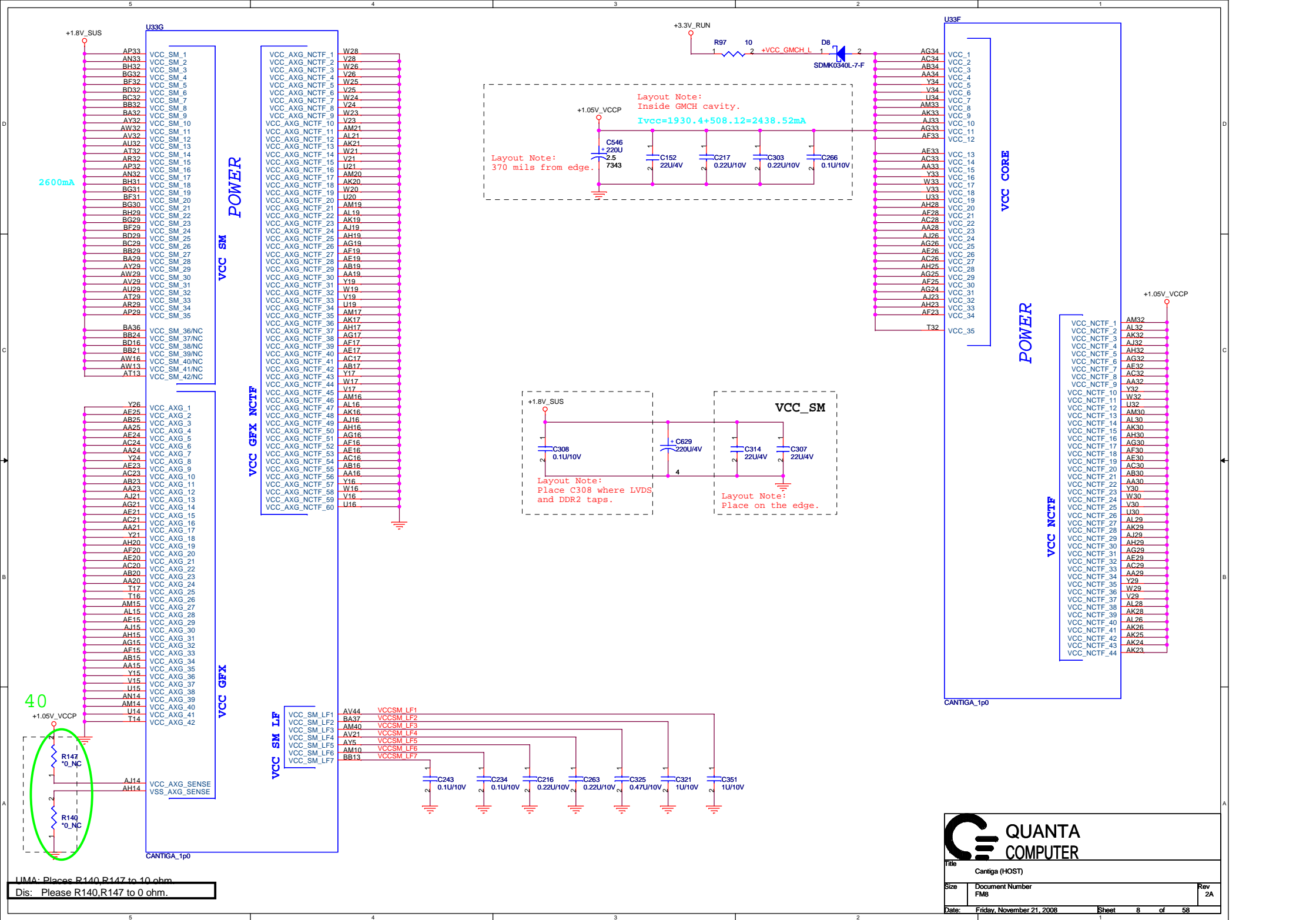


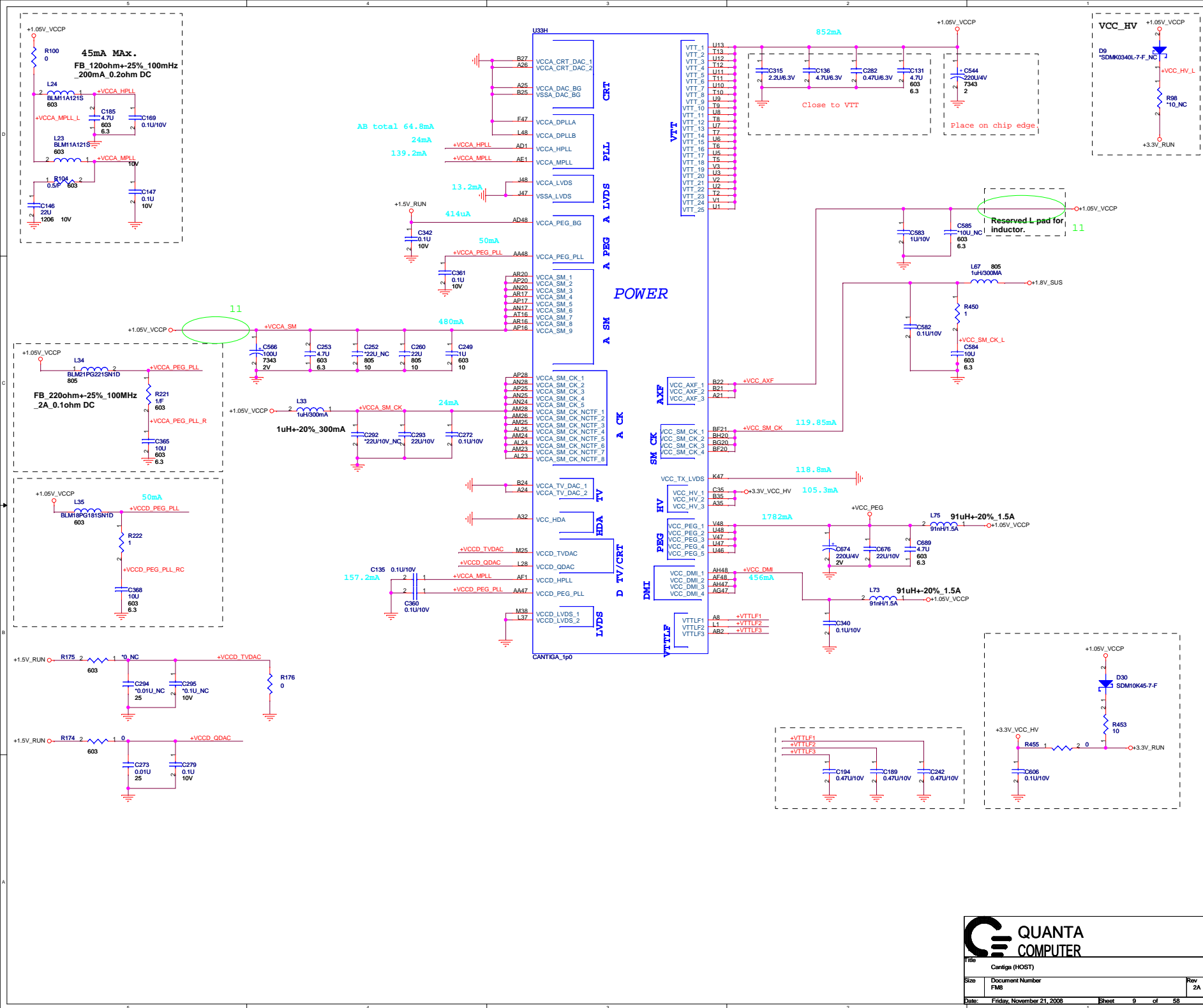
HOST

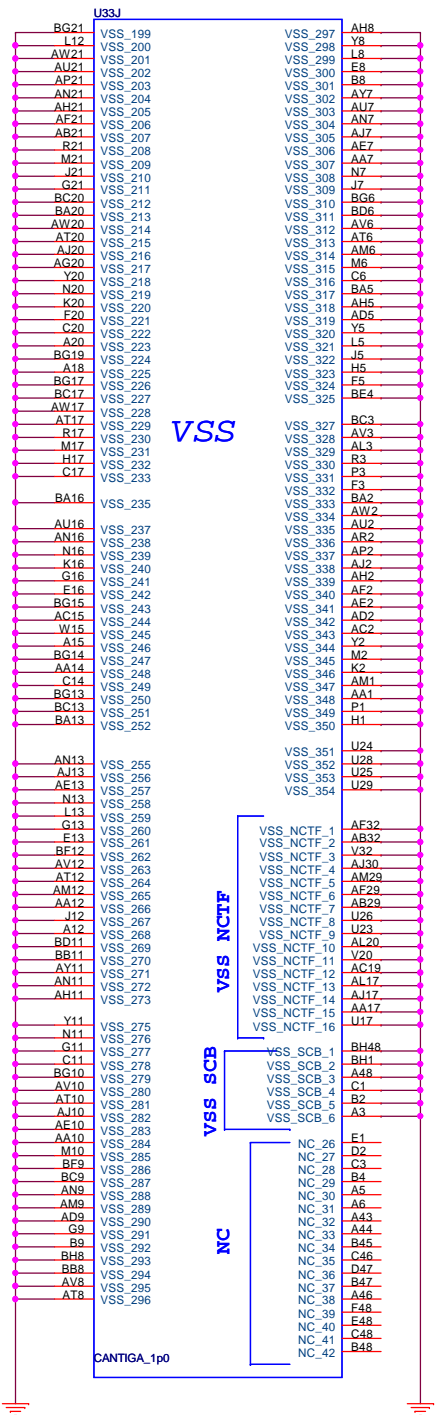
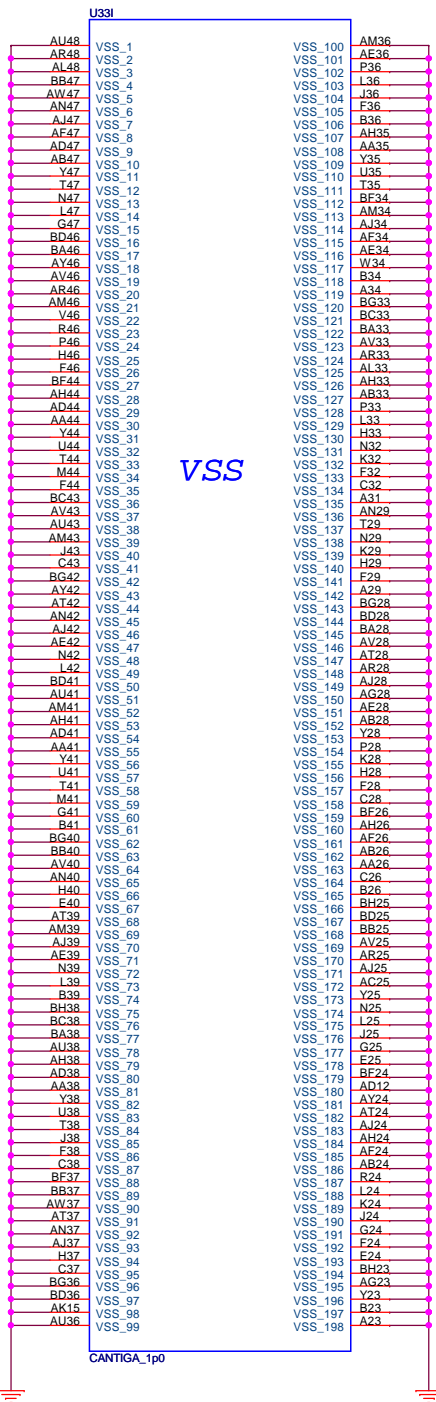





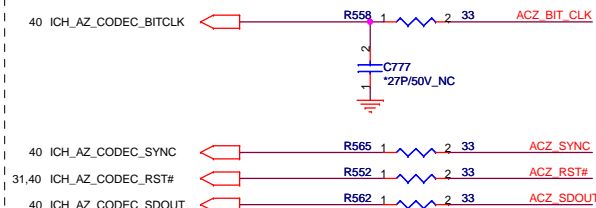
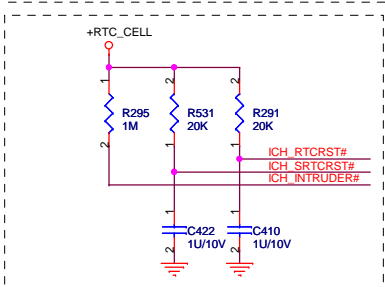
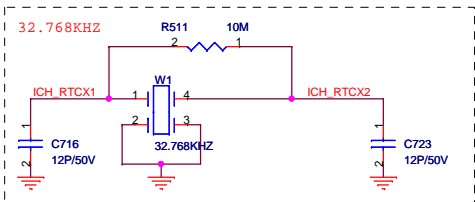




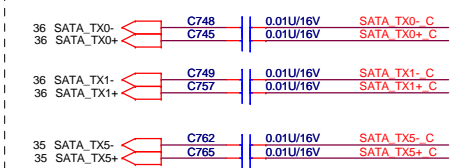




| | | |
|--|------------------------|-----------|
|  QUANTA COMPUTER | | |
| Title Cantiga (HOST) | | |
| Size FMS | Document Number FMS | Rev 2A |
| Date: Friday, November 21, 2008 | Sheet 10 | of 58 |



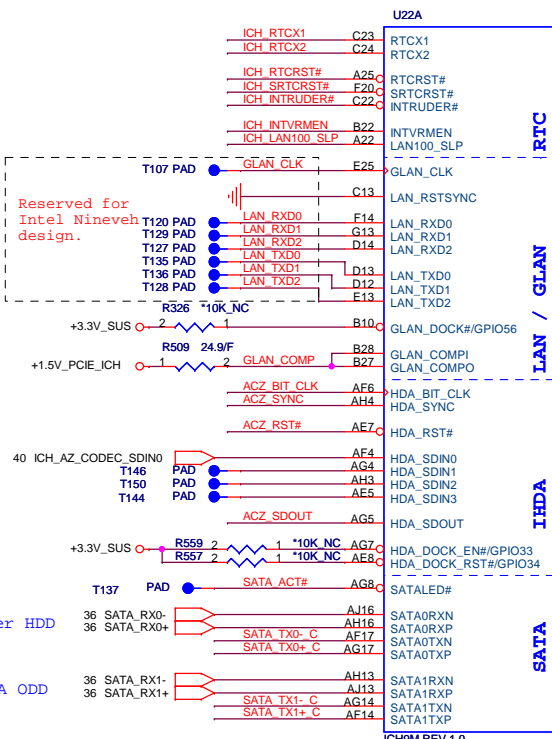
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R558, R565, R552 & R562 should equal distance to the T split trace. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

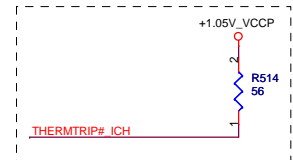
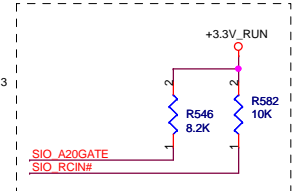
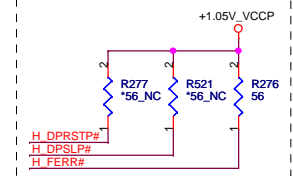
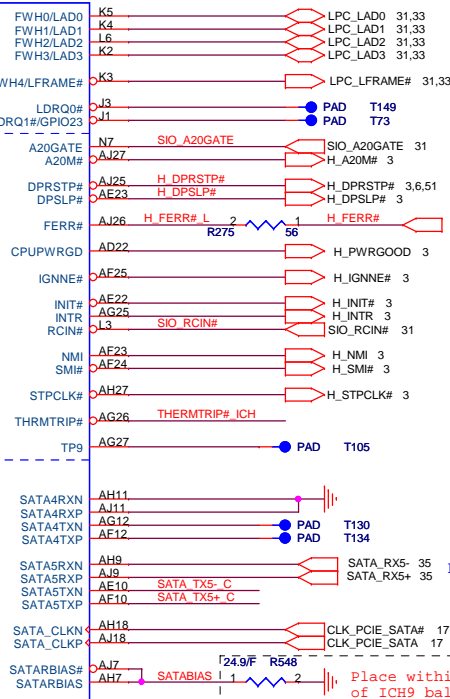
Master HDD

SATA ODD

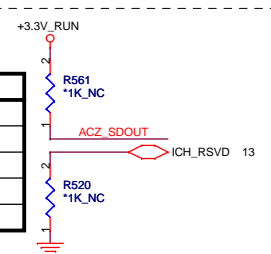


| ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5) | | |
|---|---|--|
| ICH_INTVRMEN | Low = Internal VR Disabled High = Internal VR Enabled(Default) | |
| | | |

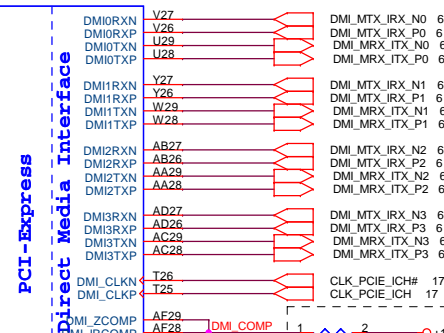
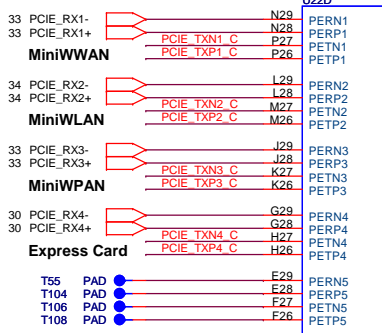
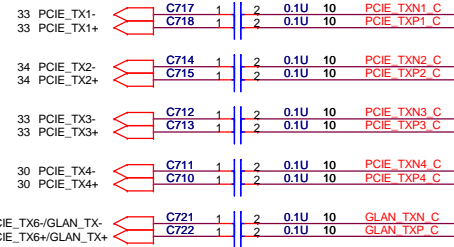
| ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05) | | |
|--|---|--|
| ICH_LAN100_SLP | Low = Internal VR Disabled High = Internal VR Enabled(Default) | |
| | | |



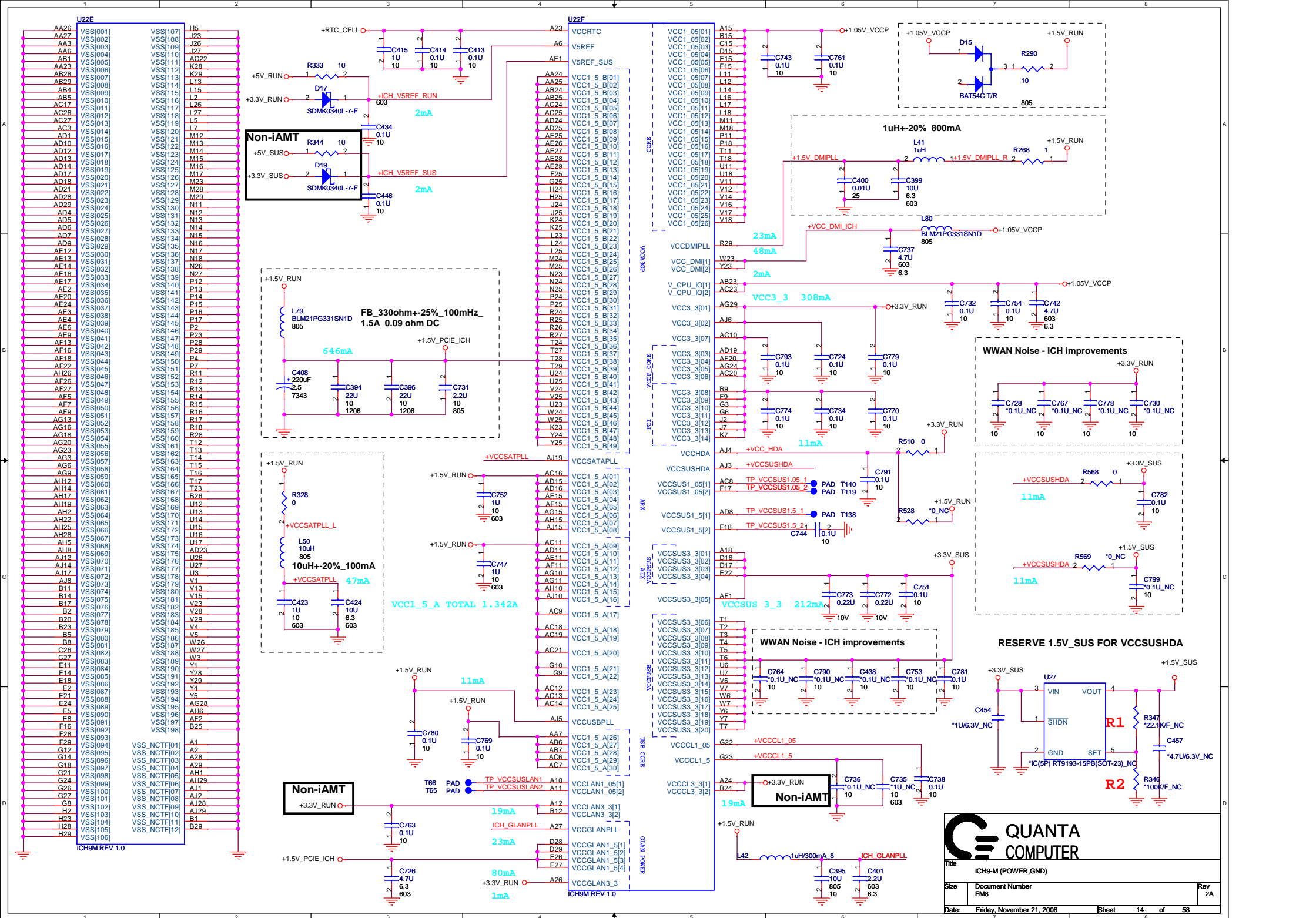
| XOR Chain Entrance Strap | | |
|--------------------------|-----------|----------------------------|
| ICH RSVD | HDA SDOUT | Description |
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal Operation (Default) |
| 1 | 1 | Set PCIE port config bit 1 |

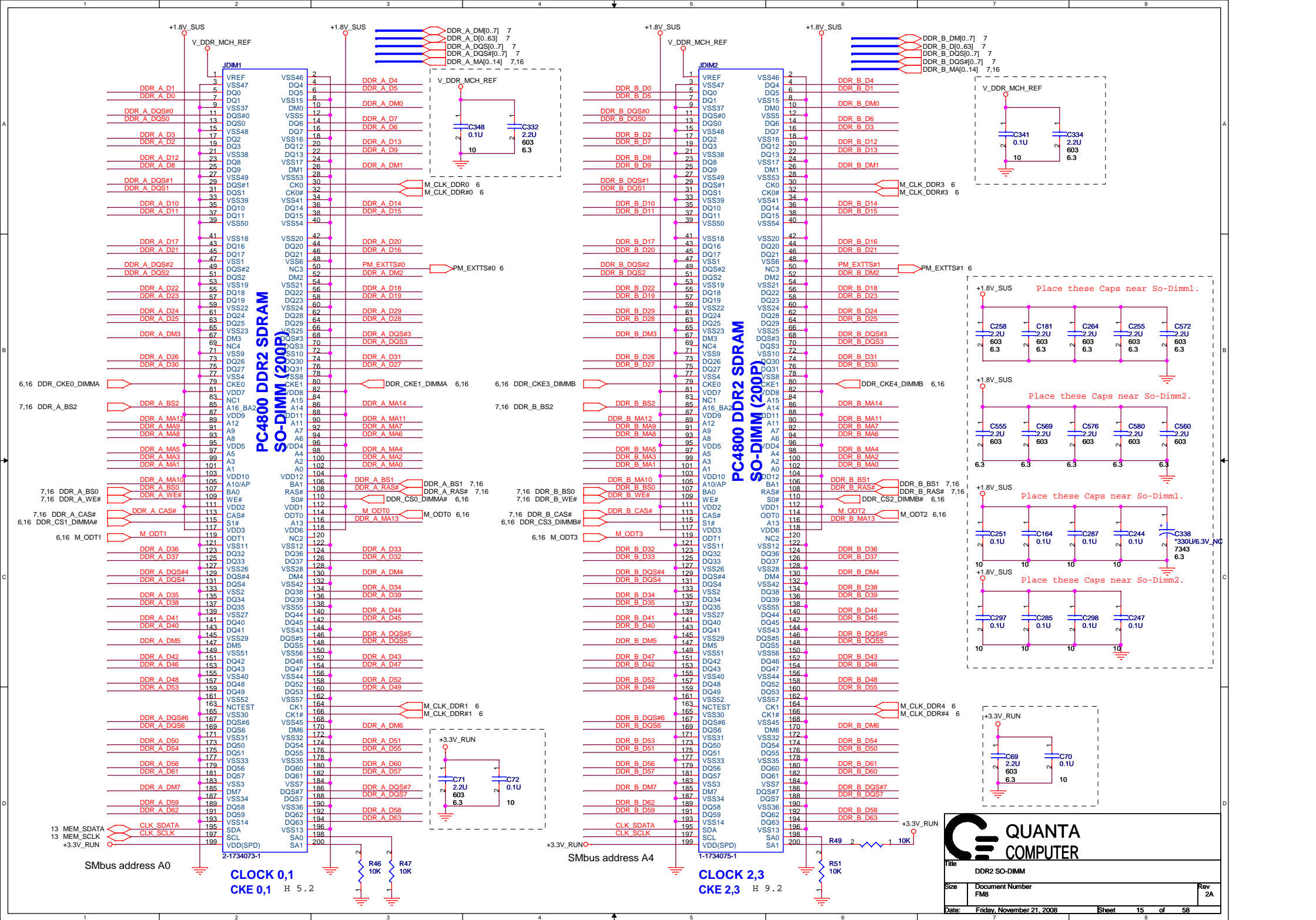


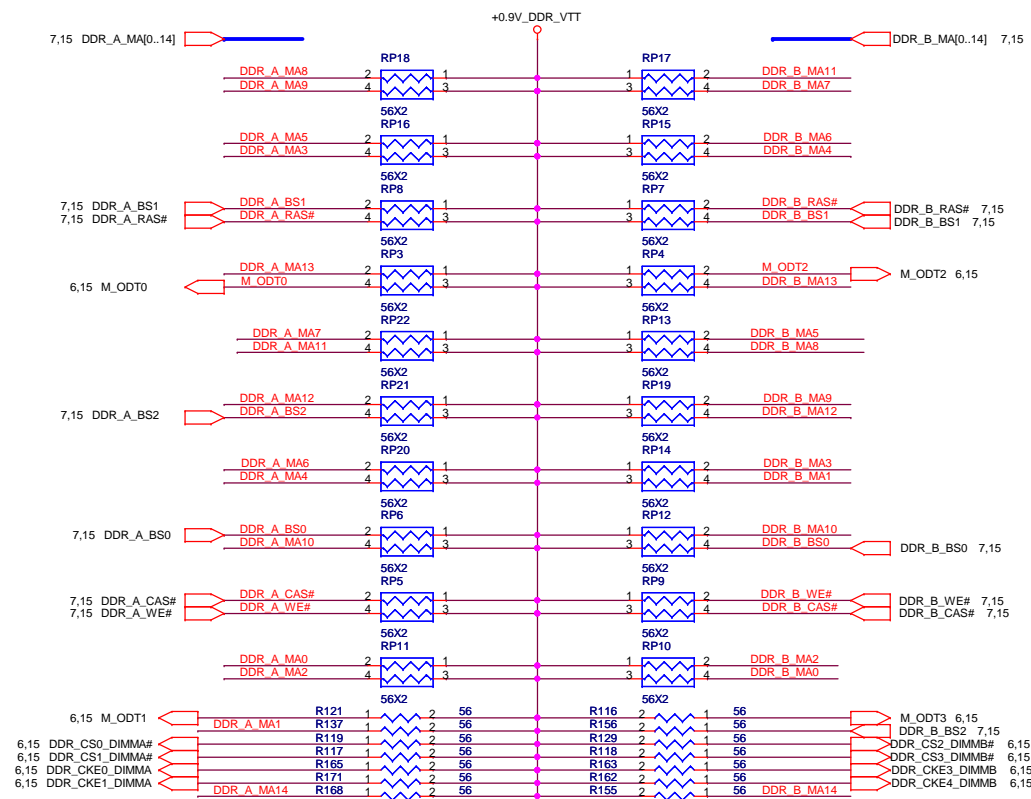
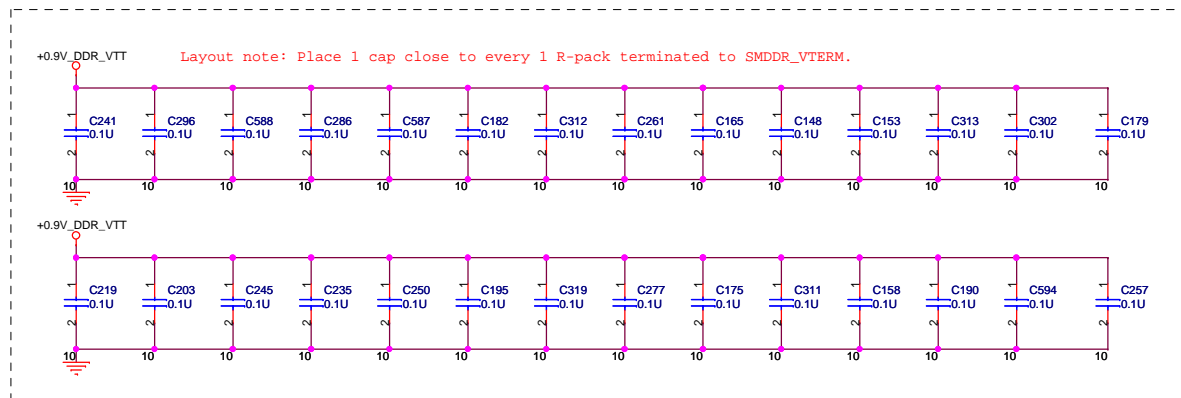
Place TX DC blocking caps close ICH9.



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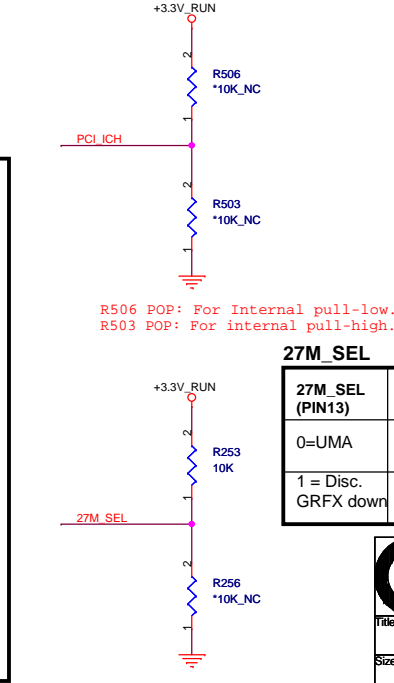
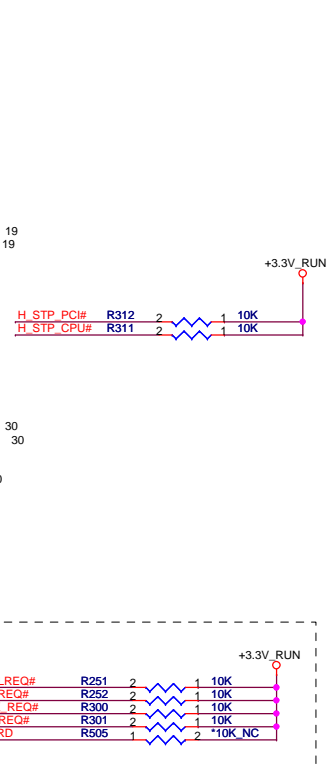
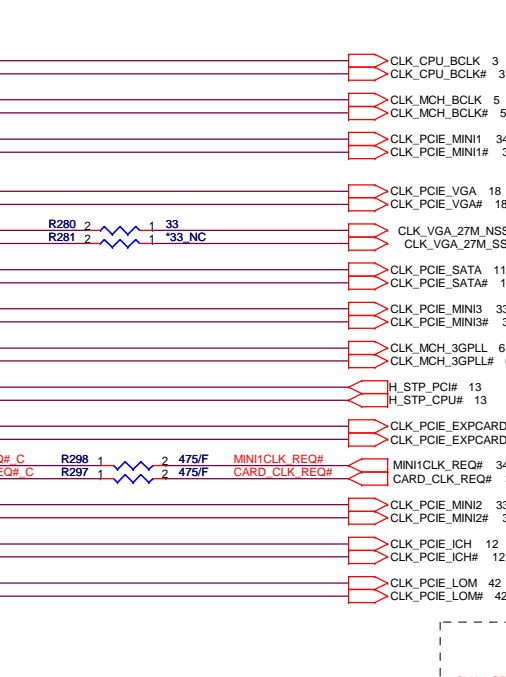
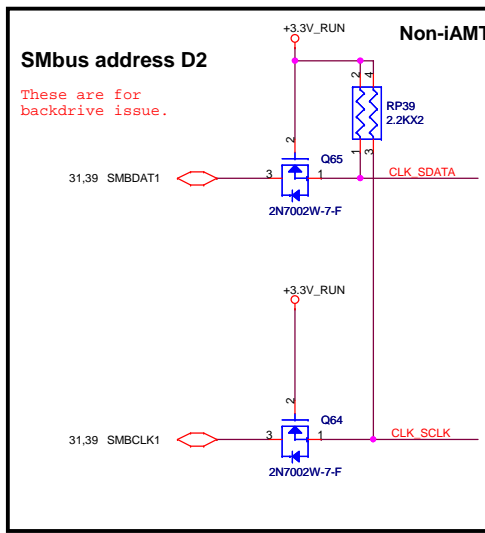
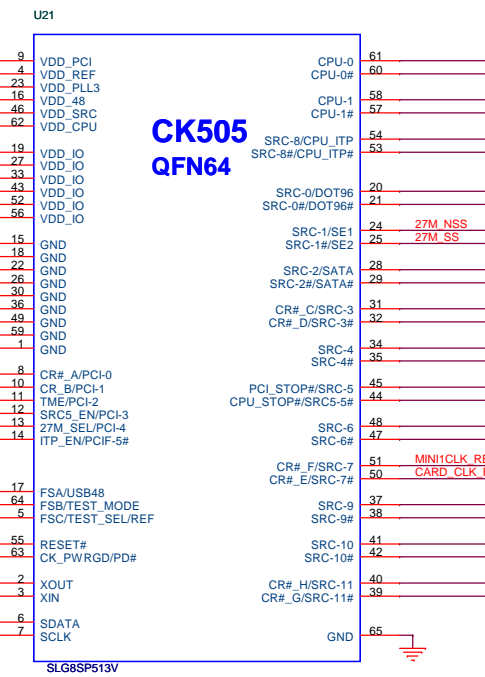
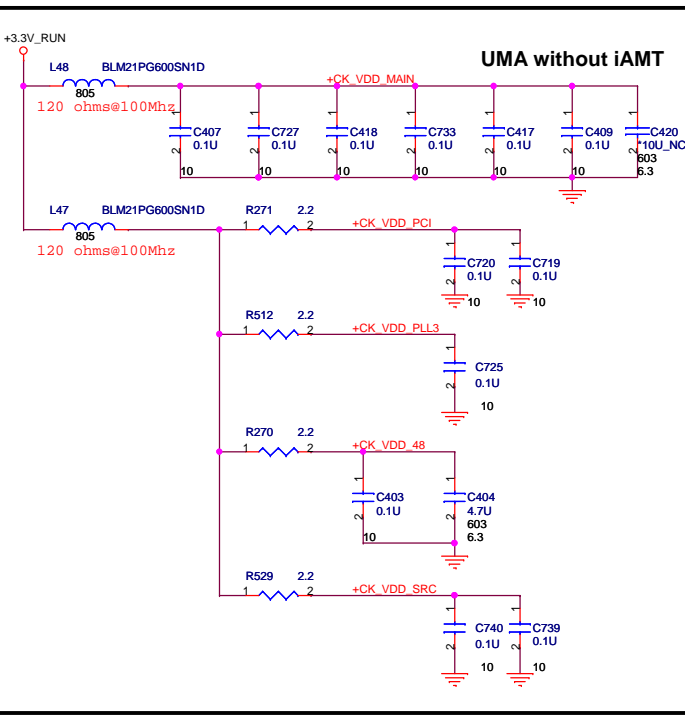
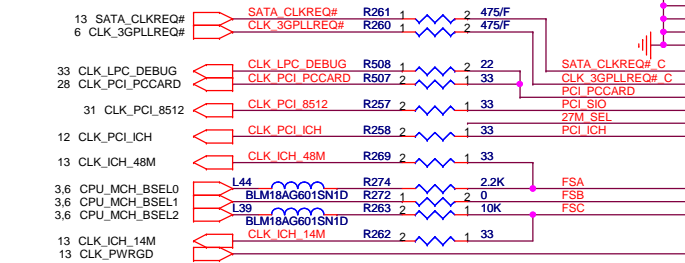
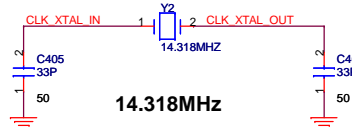
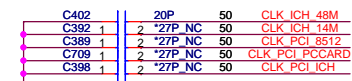




Layout notice:
Please these resistor
closely DIMMA,all
trace length<750 mil.

Layout notice:
Please these resistor
closely DIMMB,all
trace length<750 mil.

Add capacitor pads for improving WWAN.



| FSC | FSB | FSA | CPU | SRC | PCI |
|-----|-----|-----|------|-----|-----|
| 1 | 0 | 1 | 100 | 100 | 33 |
| 0 | 0 | 1 | 133 | 100 | 33 |
| 0 | 1 | 1 | 166 | 100 | 33 |
| 0 | 0 | 0 | 266 | 100 | 33 |
| 1 | 0 | 0 | 333 | 100 | 33 |
| 1 | 1 | 0 | 400 | 100 | 33 |
| 1 | 1 | 1 | RSVD | 100 | 33 |

| 27M_SEL (PIN13) | PIN20 | PIN21 | PIN24 | PIN25 |
|---------------------|--------|--------|-----------|-----------|
| 0=UMA | DOT96T | DOT96C | 96/100M_T | 96/100M_C |
| 1 = Disc. GRFX down | SRCT0 | SRCC0 | 27Mout | 27MSSout |

QUANTA COMPUTER

Title: CLOCK GENERATOR

Size: Document Number: FMB Rev: 2A

Date: Friday, November 21, 2008 Sheet: 17 of 58

6 PCIE_MTX_GRX_P0..15]
6 PCIE_MTX_GRX_N0..15]

PCIE_MTX_GRX_P0 AF30 PCIE_RX0P
PCIE_MTX_GRX_N0 AE31 PCIE_RX0N
PCIE_MTX_GRX_P1 AE29 PCIE_RX1P
PCIE_MTX_GRX_N1 AD28 PCIE_RX1N
PCIE_MTX_GRX_P2 AD30 PCIE_RX2P
PCIE_MTX_GRX_N2 AC31 PCIE_RX2N
PCIE_MTX_GRX_P3 AC29 PCIE_RX3P
PCIE_MTX_GRX_N3 AB28 PCIE_RX3N
PCIE_MTX_GRX_P4 AB30 PCIE_RX4P
PCIE_MTX_GRX_N4 AA31 PCIE_RX4N
PCIE_MTX_GRX_P5 AA29 PCIE_RX5P
PCIE_MTX_GRX_N5 Y28 PCIE_RX5N
PCIE_MTX_GRX_P6 Y30 PCIE_RX6P
PCIE_MTX_GRX_N6 W31 PCIE_RX6N
PCIE_MTX_GRX_P7 W28 PCIE_RX7P
PCIE_MTX_GRX_N7 V28 PCIE_RX7N
PCIE_MTX_GRX_P8 V30 PCIE_RX8P
PCIE_MTX_GRX_N8 U31 PCIE_RX8N
PCIE_MTX_GRX_P9 U29 PCIE_RX9P
PCIE_MTX_GRX_N9 T28 PCIE_RX9N
PCIE_MTX_GRX_P10 T30 PCIE_RX10P
PCIE_MTX_GRX_N10 R31 PCIE_RX10N
PCIE_MTX_GRX_P11 R29 PCIE_RX11P
PCIE_MTX_GRX_N11 P28 PCIE_RX11N
PCIE_MTX_GRX_P12 P30 PCIE_RX12P
PCIE_MTX_GRX_N12 N31 PCIE_RX12N
PCIE_MTX_GRX_P13 N29 PCIE_RX13P
PCIE_MTX_GRX_N13 M28 PCIE_RX13N
PCIE_MTX_GRX_P14 M30 PCIE_RX14P
PCIE_MTX_GRX_N14 L31 PCIE_RX14N
PCIE_MTX_GRX_P15 L29 PCIE_RX15P
PCIE_MTX_GRX_N15 K30 PCIE_RX15N

PCI-EXPRESS INTERFACE

PCIE_TX0P AH30 PCIE_MRX_GTX_C_P0
PCIE_TX0N AG31 PCIE_MRX_GTX_C_N0
PCIE_TX1P AG29 PCIE_MRX_GTX_C_P1
PCIE_TX1N AF28 PCIE_MRX_GTX_C_N1
PCIE_TX2P AF27 PCIE_MRX_GTX_C_P2
PCIE_TX2N AF26 PCIE_MRX_GTX_C_N2
PCIE_TX3P AD27 PCIE_MRX_GTX_C_P3
PCIE_TX3N AD26 PCIE_MRX_GTX_C_N3
PCIE_TX4P AC25 PCIE_MRX_GTX_C_P4
PCIE_TX4N AB25 PCIE_MRX_GTX_C_N4
PCIE_TX5P Y23 PCIE_MRX_GTX_C_P5
PCIE_TX5N Y24 PCIE_MRX_GTX_C_N5
PCIE_TX6P AB27 PCIE_MRX_GTX_C_P6
PCIE_TX6N AB26 PCIE_MRX_GTX_C_N6
PCIE_TX7P Y27 PCIE_MRX_GTX_C_P7
PCIE_TX7N Y26 PCIE_MRX_GTX_C_N7
PCIE_TX8P W24 PCIE_MRX_GTX_C_P8
PCIE_TX8N W23 PCIE_MRX_GTX_C_N8
PCIE_TX9P V27 PCIE_MRX_GTX_C_P9
PCIE_TX9N U26 PCIE_MRX_GTX_C_N9
PCIE_TX10P U24 PCIE_MRX_GTX_C_P10
PCIE_TX10N U23 PCIE_MRX_GTX_C_N10
PCIE_TX11P T26 PCIE_MRX_GTX_C_P11
PCIE_TX11N T27 PCIE_MRX_GTX_C_N11
PCIE_TX12P T24 PCIE_MRX_GTX_C_P12
PCIE_TX12N T23 PCIE_MRX_GTX_C_N12
PCIE_TX13P P27 PCIE_MRX_GTX_C_P13
PCIE_TX13N P26 PCIE_MRX_GTX_C_N13
PCIE_TX14P P24 PCIE_MRX_GTX_C_P14
PCIE_TX14N P23 PCIE_MRX_GTX_C_N14
PCIE_TX15P M27 PCIE_MRX_GTX_C_P15
PCIE_TX15N M26 PCIE_MRX_GTX_C_N15

6 PCIE_MRX_GTX_P0..15]
6 PCIE_MRX_GTX_N0..15]

PCIE_MRX_GTX_P0 0.1U 2 1 C814 10 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C815 10 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C816 10 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C817 10 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C818 10 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C819 10 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C820 10 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C821 10 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C822 10 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C823 10 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C824 10 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C825 10 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C826 10 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C827 10 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C828 10 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C829 10 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U 2 1 C830 10 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C831 10 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C832 10 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C833 10 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C834 10 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C835 10 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C836 10 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C837 10 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C838 10 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C839 10 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C840 10 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C841 10 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C842 10 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C843 10 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C844 10 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C845 10 PCIE_MRX_GTX_C_N15

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

17 CLK_PCIE_VGA AK30
17 CLK_PCIE_VGA# AK32
13 PLTRST_DELAY# AL27
6,12,30,31,33,34,42 PLTRST# M92-S2M92-XT

43

(1.1V)
+PCIE_VDDC

M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)

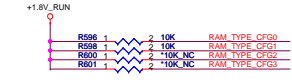
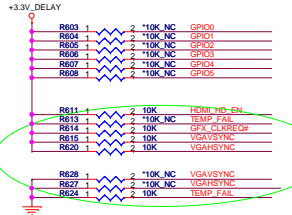


Table with 3 columns: Title, Size, Date. Title: VGA-M92-XT (PCIe). Size: Document Number FM8. Date: Friday, November 21, 2008. Sheet 18 of 58.

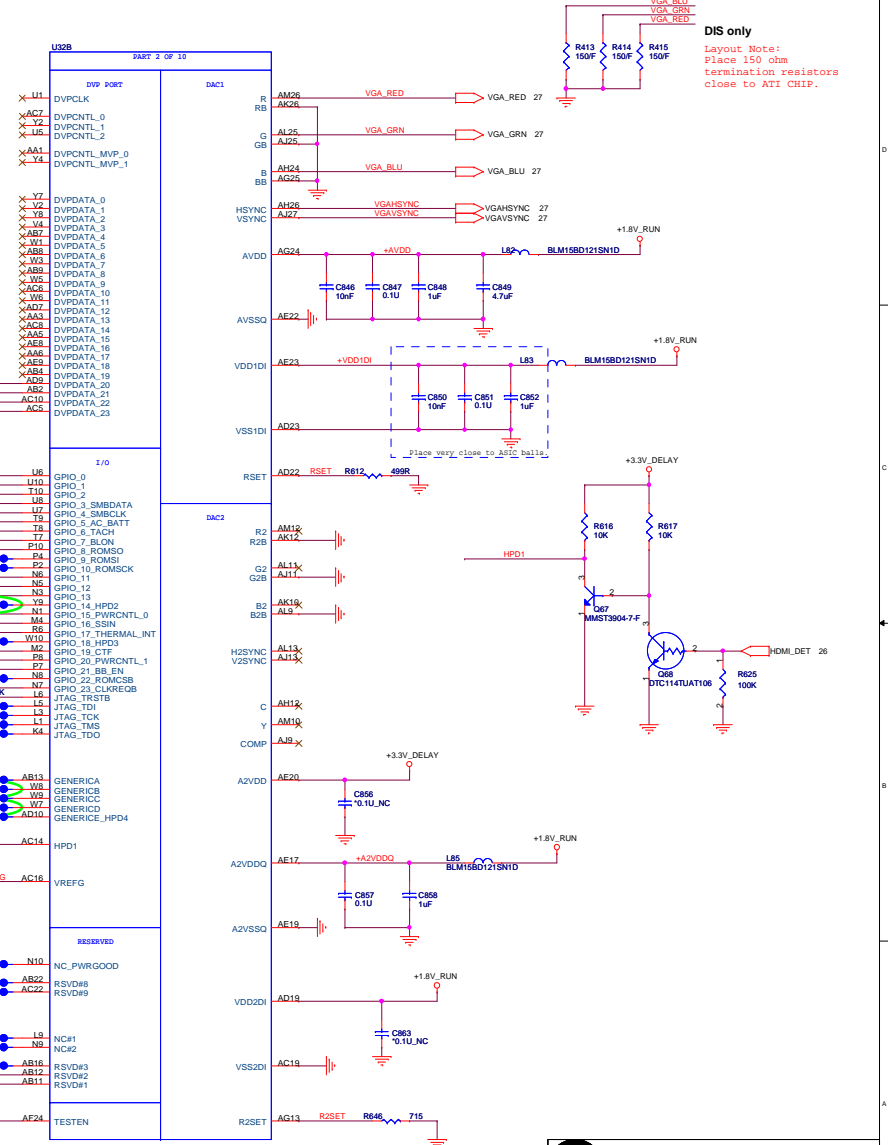
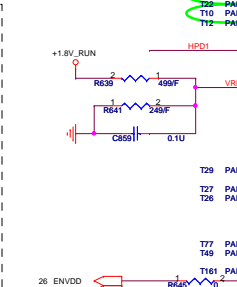
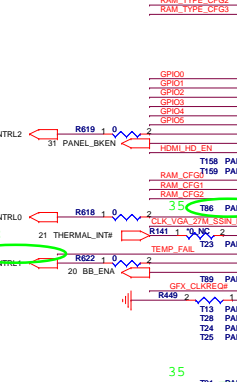
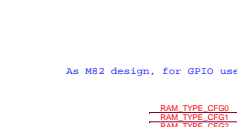
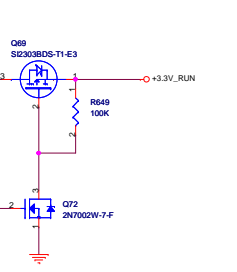
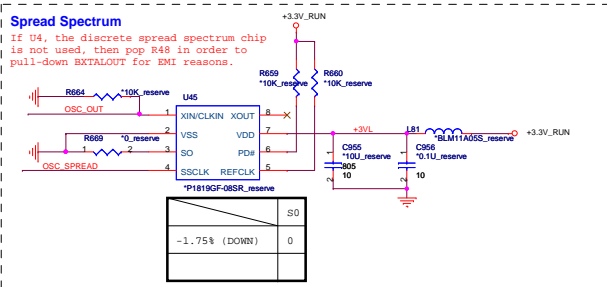
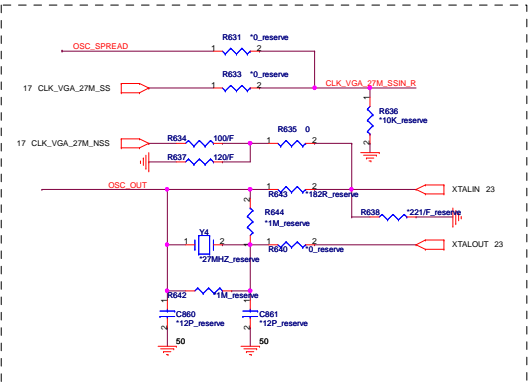
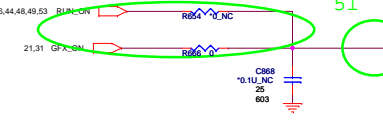
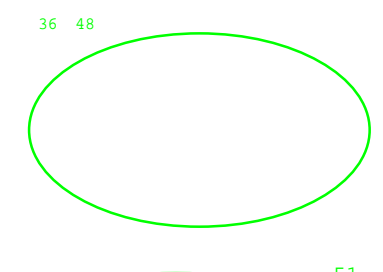
| MEMORY APERTURE SIZE SELECT | | | | |
|-----------------------------|---------------|----------------|----------------|----------------|
| MEMORY SIZE | CFG3 GP109 | CFG2 GP1013 | CFG1 GP1012 | CFG0 GP1011 |
| 128MB | | 0 | 0 | 0 |
| 256MB | | 0 | 0 | 1 |
| 64MB | | 0 | 1 | 0 |
| 512MB | | 1 | 0 | 0 |



| GPIO Straps table | DESCRIPTION OF DEFAULT SETTINGS | FMS setting |
|-------------------|---|-------------|
| GPIO0 | GPIO0 - TX, PWRB_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop) | 0 |
| GPIO1 | GPIO1 - TX, DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop) | 0 |
| GPIO2 | GPIO2 - BUF, GEN2_EN (5.0 GT/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2 | 0 |
| GPIO3 | ATI reserved configuration straps. | 0 |
| GPIO4 | ATI reserved configuration straps. | 0 |
| GPIO5 | GPIO_5_AC_BATT 0: Battery saving mode = 0.9V 1: AC (Performance mode) = 3.3V | 0 |
| GPIO6 | ATI Internal use only | 0 |



| Memory Straps | RAM_TYPE | RAM_TYPE | RAM_TYPE | RAM_TYPE | Quanta PN (QuantaBuy) | Quanta PN (WinBuy) | Vendor PN | 31 level PN |
|-----------------------|----------|----------|----------|----------|-----------------------|--------------------|------------------|-------------|
| CFG3 | CFG2 | CFG1 | CFG0 | | | | | |
| 800MHz | | | | | AKD5LWGT501 | AKD5LWGT504 | K4J10324QD-HC12 | 31FM8MB0030 |
| 512MB(32M*32) Samsung | 0 | 0 | 1 | 0 | | | | |
| 900MHz | | | | | AKD5LWFT*03 | AKD5LWFT*00 | HYB18H1G321AF-11 | 31FM8MB0000 |
| 512MB(32M*32) Qimonda | 0 | 0 | 1 | 1 | | | | |
| 800MHz | | | | | AKD5FWGT500 | AKD5FWGT503 | K4J52324QH-HC12 | 31FM8MB0040 |
| 256MB(16M*32) Samsung | 0 | 0 | 0 | 1 | | | | |
| 800MHz | | | | | AKD5FWHTW03 | AKD5FWHTW06 | H5RS5223CFR-11C | 31FM8MB0020 |
| 256MB(16M*32) Hynix | 0 | 0 | 0 | 0 | | | | |



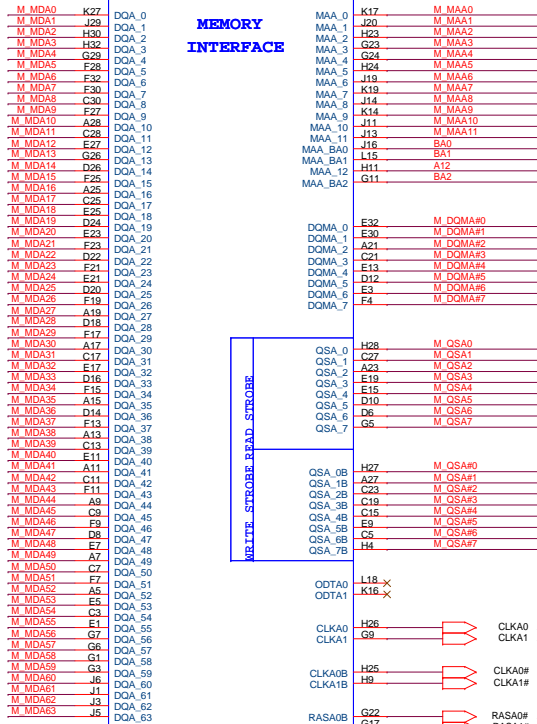
| | | | |
|-----------------|---------------------------|-------|----------|
| QUANTA COMPUTER | | | |
| Part | VGA-MB2-KT (PCIe) | Rev | 2A |
| Size | Document Number | | |
| FMS | | | |
| Date | Friday, November 21, 2008 | Sheet | 19 of 58 |



MEMORY INTERFACE

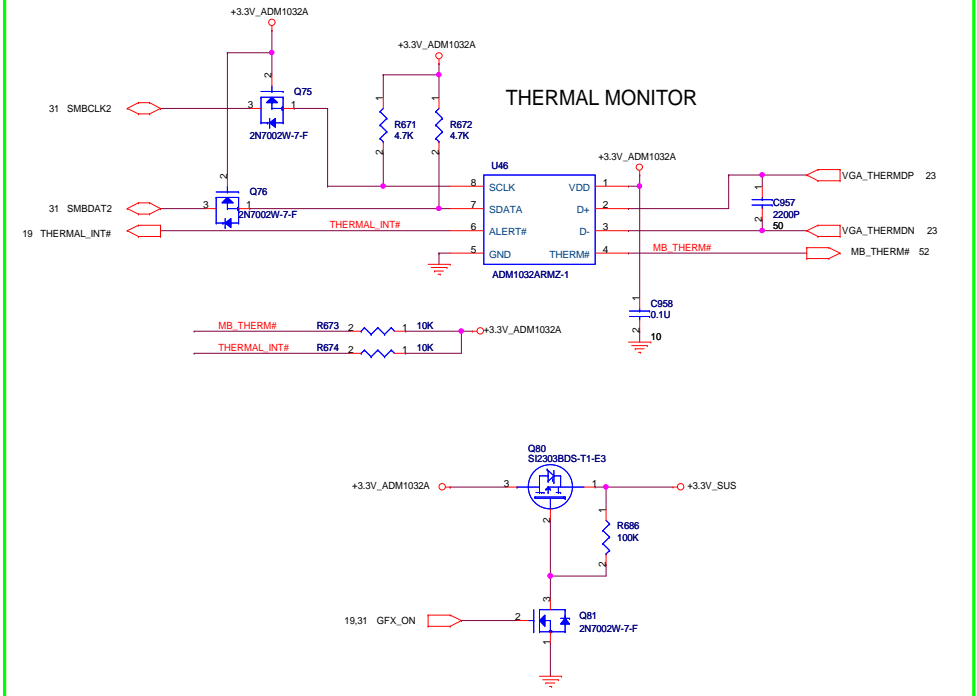
U32C

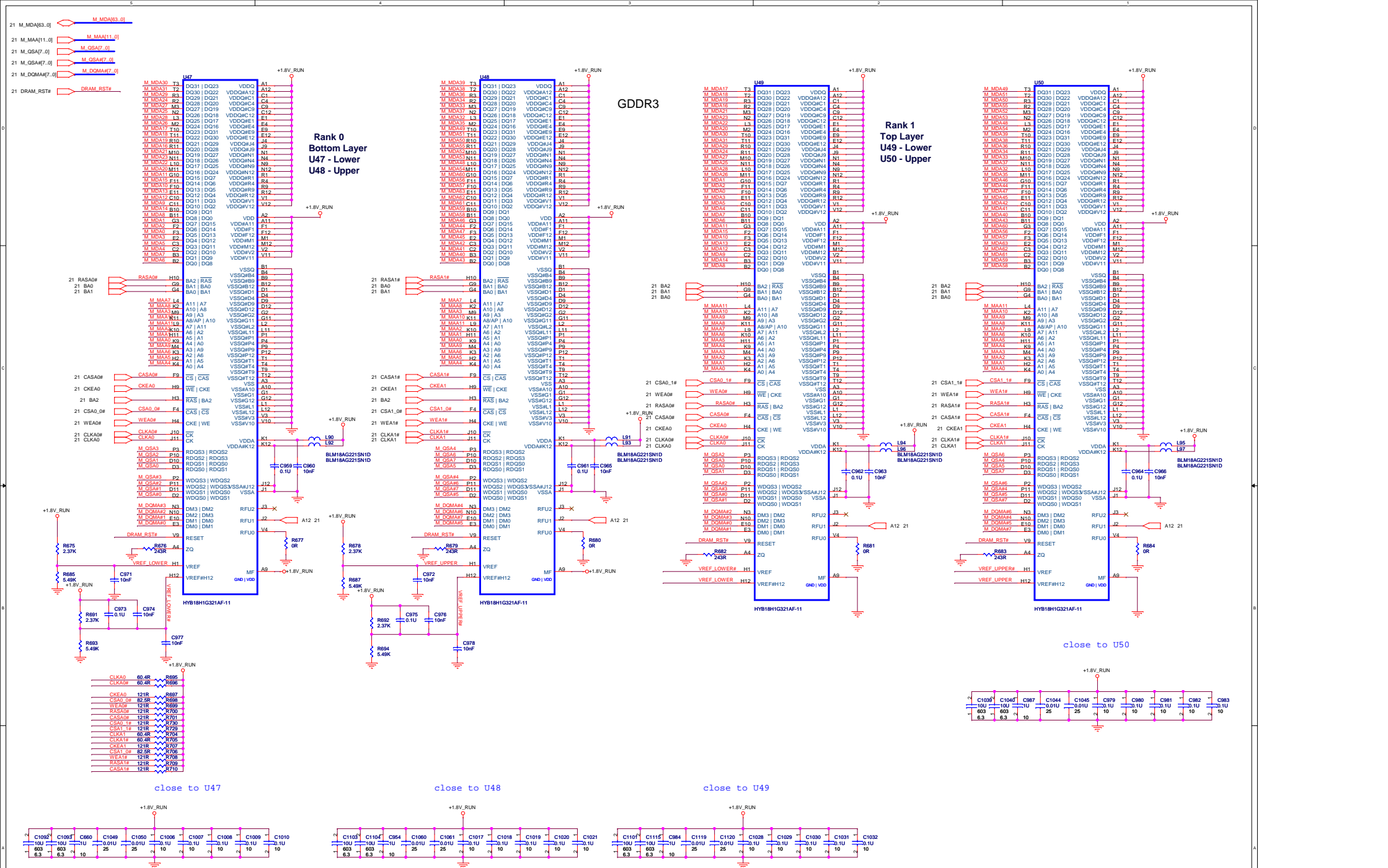
MEMORY INTERFACE



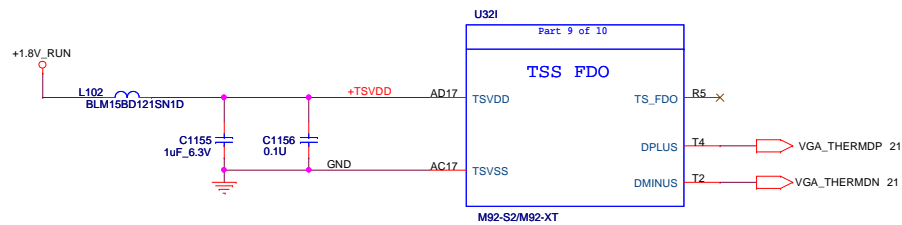
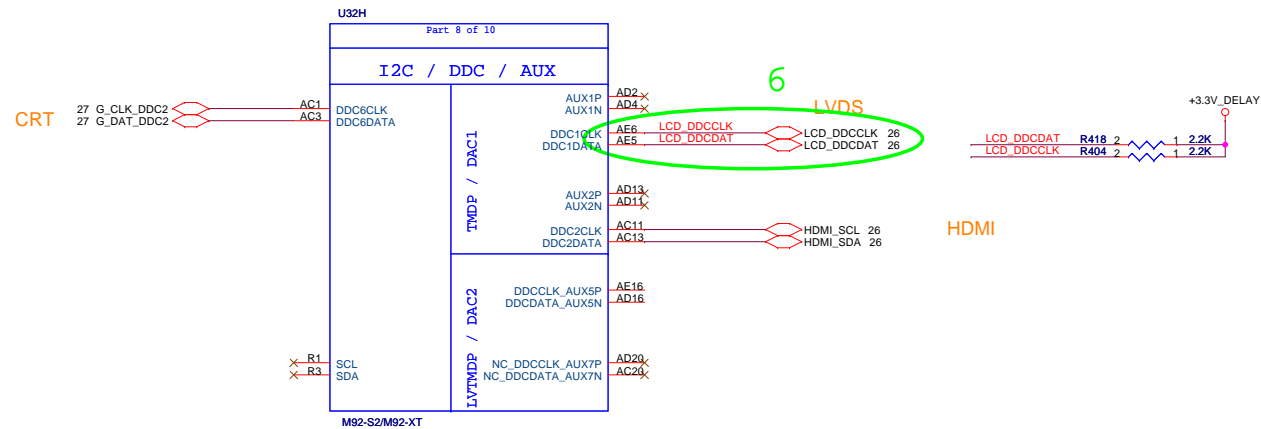
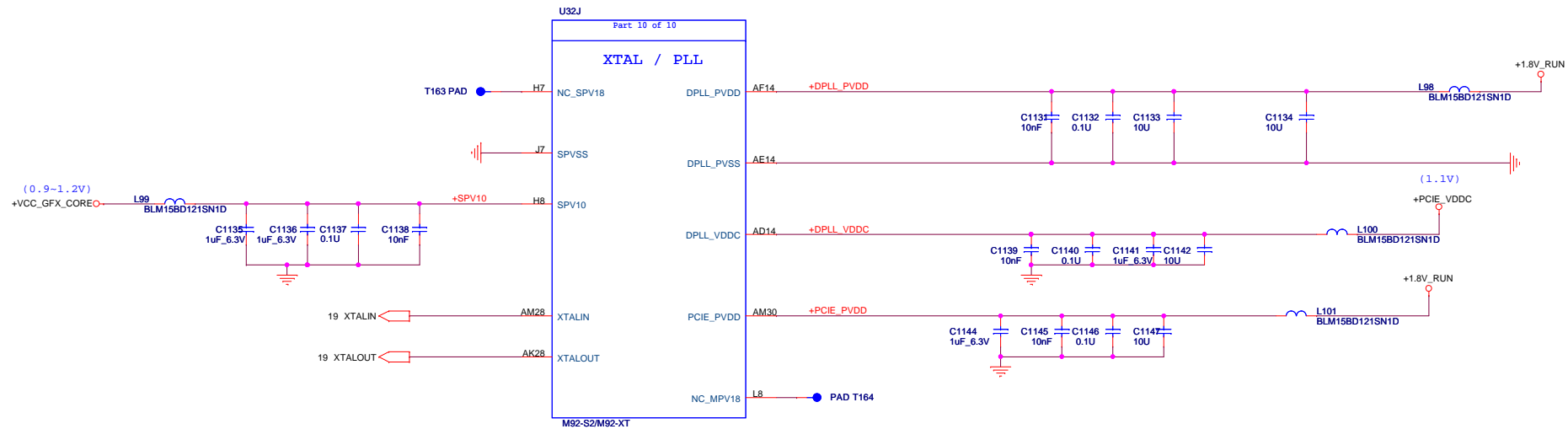
36 42 47

M92 thermal monitor change external to internal. 10/20

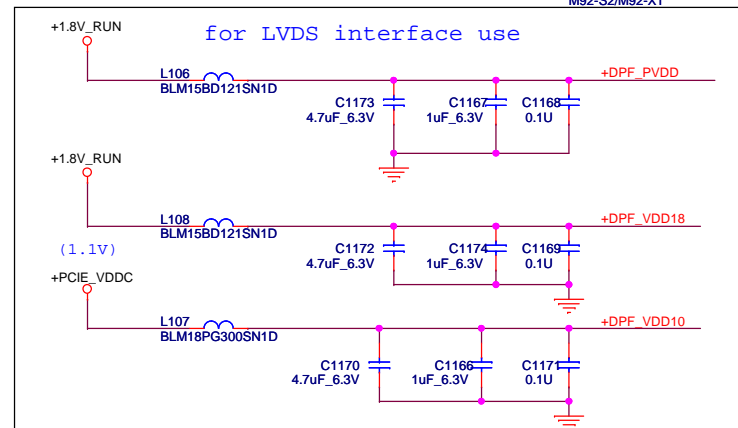
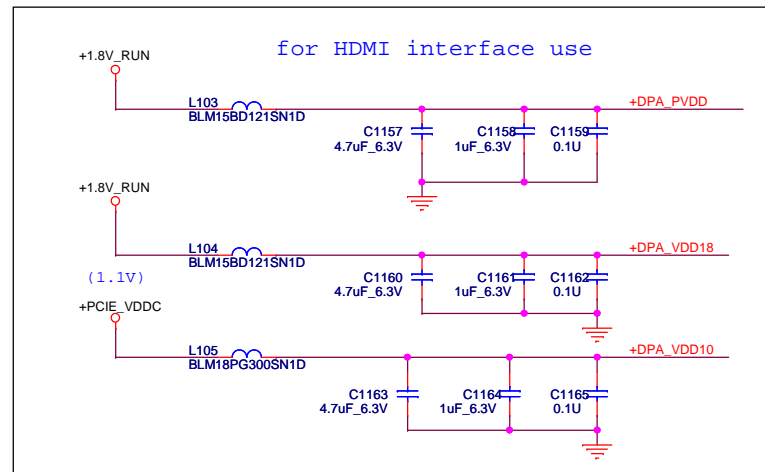
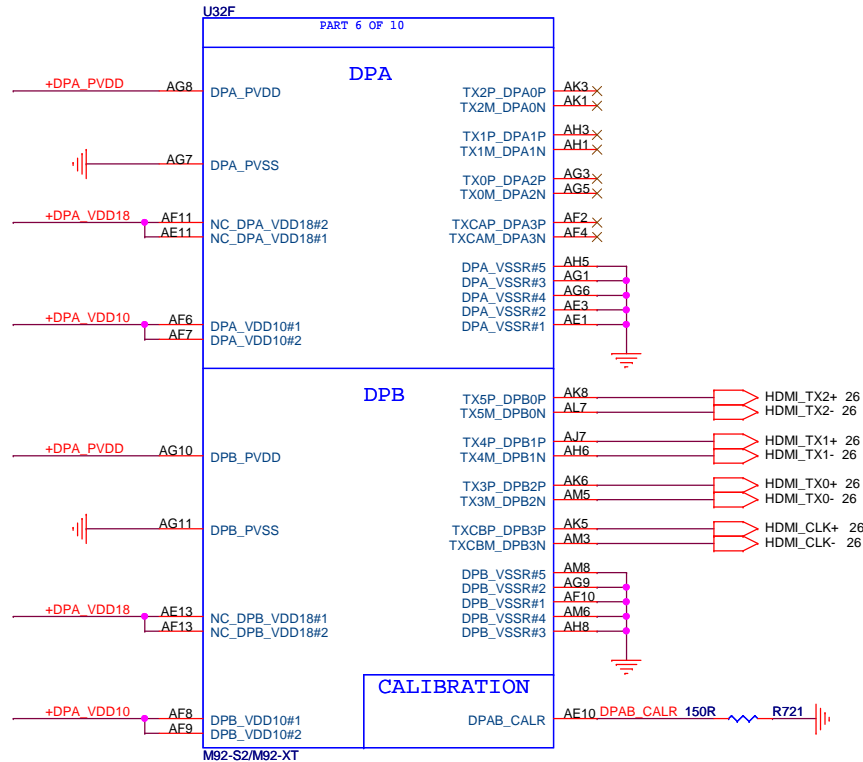




Base on M82 GDDR Caps.



TMDP(HDMI) INTERFACE





| Title |
|-------|
|-------|

VGA-M82-S (PCIe)

Size

| |
|------------------------|
| Document Number FM8 |
|------------------------|

Rev

2A

Date:

Friday, November 21, 2008

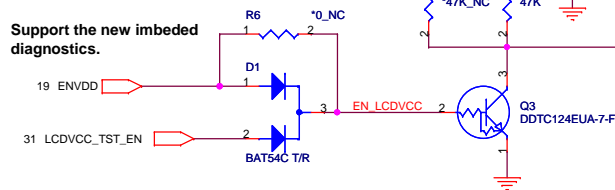
Sheet

25

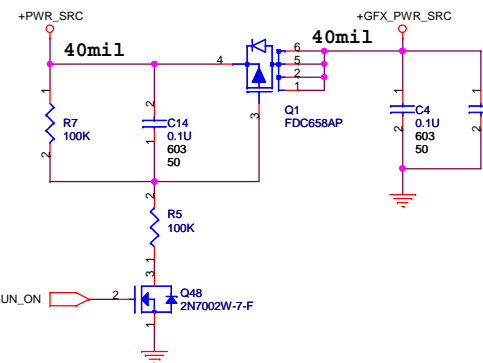
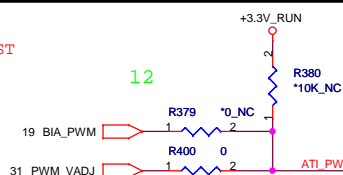
of

58

Support the new imbedded diagnostics.



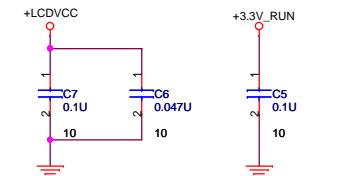
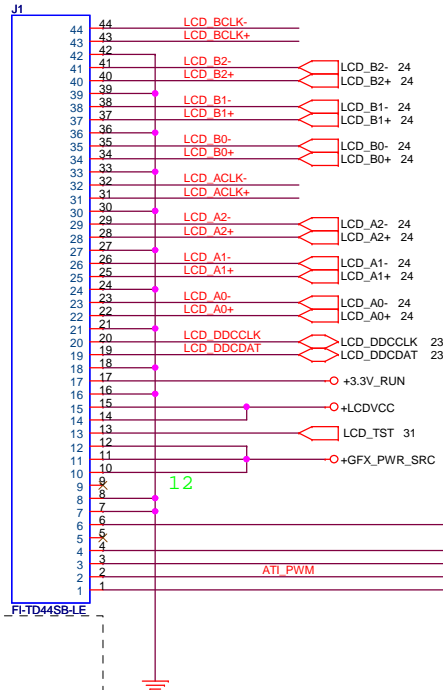
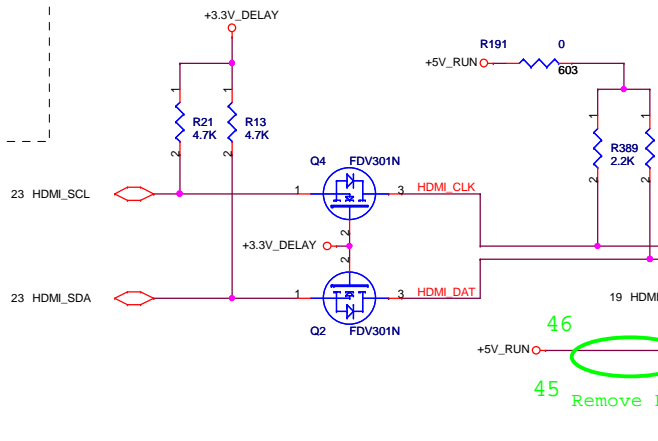
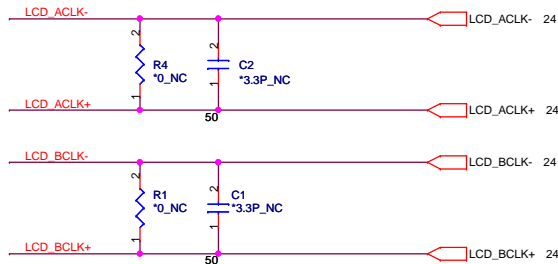
Populate R379 for DPST implementation only.



| | | | |
|--------------|-----|--------------|-------------|
| 24 HDMI_TX2+ | C25 | 0.1U/10V/X7R | HDMI TX2+ R |
| 24 HDMI_TX2- | C26 | 0.1U/10V/X7R | HDMI TX2- R |
| 24 HDMI_TX1+ | C23 | 0.1U/10V/X7R | HDMI TX1+ R |
| 24 HDMI_TX1- | C22 | 0.1U/10V/X7R | HDMI TX1- R |
| 24 HDMI_TX0+ | C27 | 0.1U/10V/X7R | HDMI TX0+ R |
| 24 HDMI_TX0- | C30 | 0.1U/10V/X7R | HDMI TX0- R |
| 24 HDMI_CLK+ | C21 | 0.1U/10V/X7R | HDMI CLK+ R |
| 24 HDMI_CLK- | C20 | 0.1U/10V/X7R | HDMI CLK- R |

Shunt capacitors on LVDS for improving WWAN.

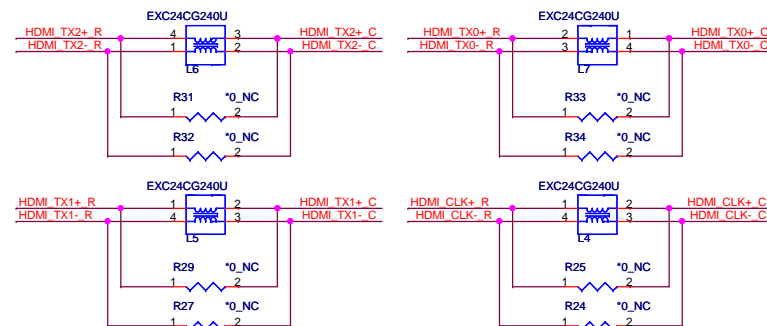
| | | | | | | |
|---------|-----|---|---|----------|----|---------|
| LCD B0- | C16 | 1 | 2 | *3.3P NC | 50 | LCD B0+ |
| LCD B1- | C10 | 1 | 2 | *3.3P NC | 50 | LCD B1+ |
| LCD B2- | C15 | 1 | 2 | *3.3P NC | 50 | LCD B2+ |
| LCD A0- | C13 | 1 | 2 | *3.3P NC | 50 | LCD A0+ |
| LCD A1- | C12 | 1 | 2 | *3.3P NC | 50 | LCD A1+ |
| LCD A2- | C3 | 1 | 2 | *3.3P NC | 50 | LCD A2+ |



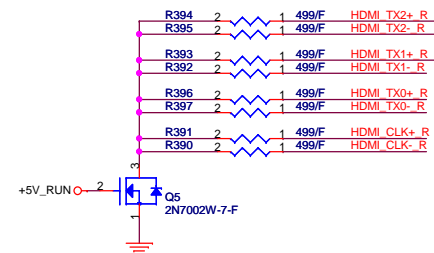
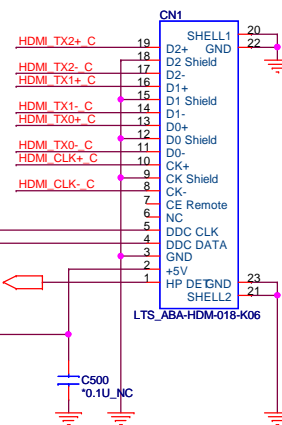
Address : A9H --Contrast
AAH --Backlight

(3)08/22: delete SM Bus and add contrast function

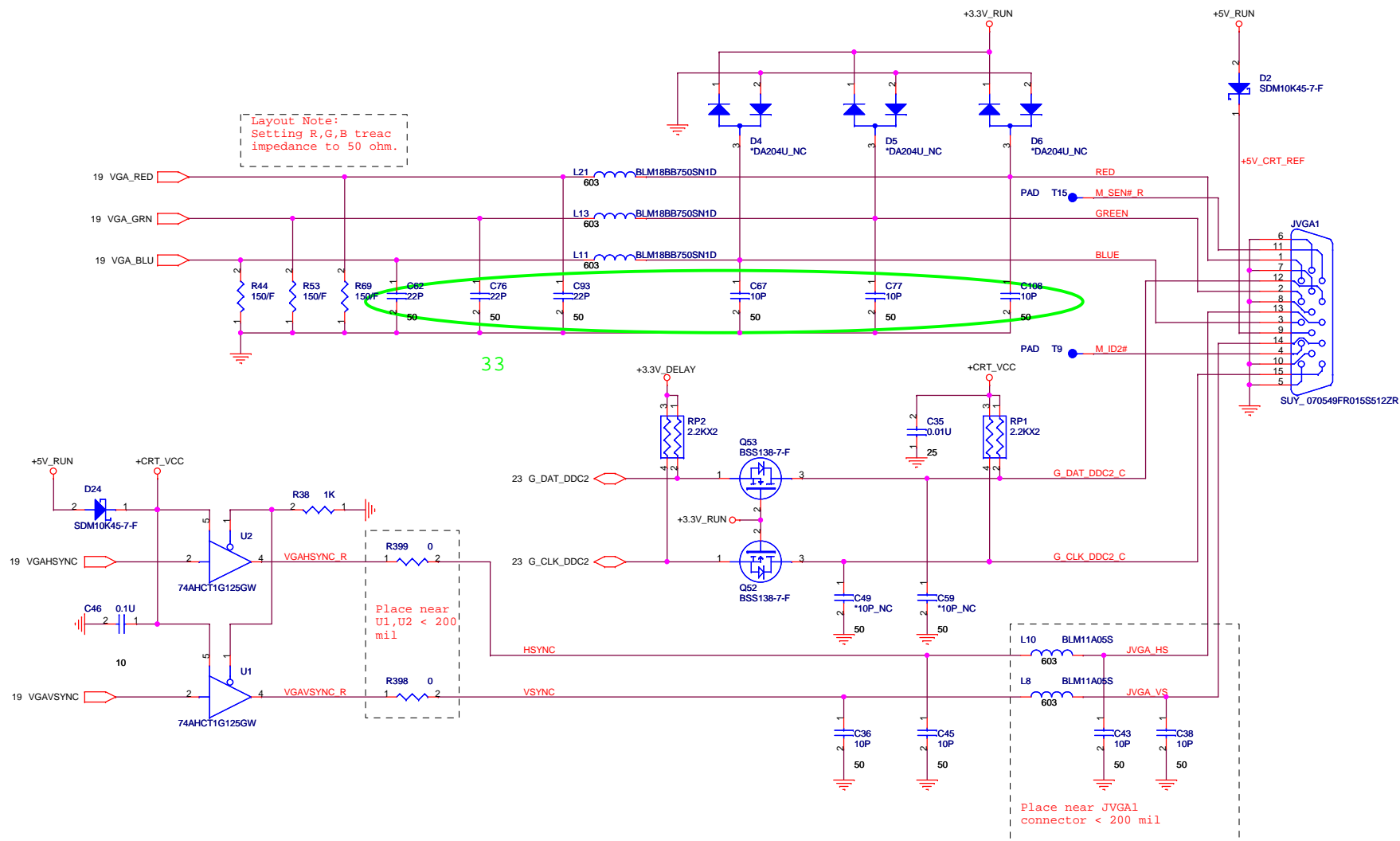
| | |
|-------------------|----|
| LCD_CONTRAST | 31 |
| INVERTER_CBL_DET# | 31 |
| LCD_BAK# | 31 |
| LCD_CBL_DET# | 31 |



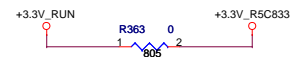
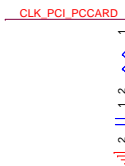
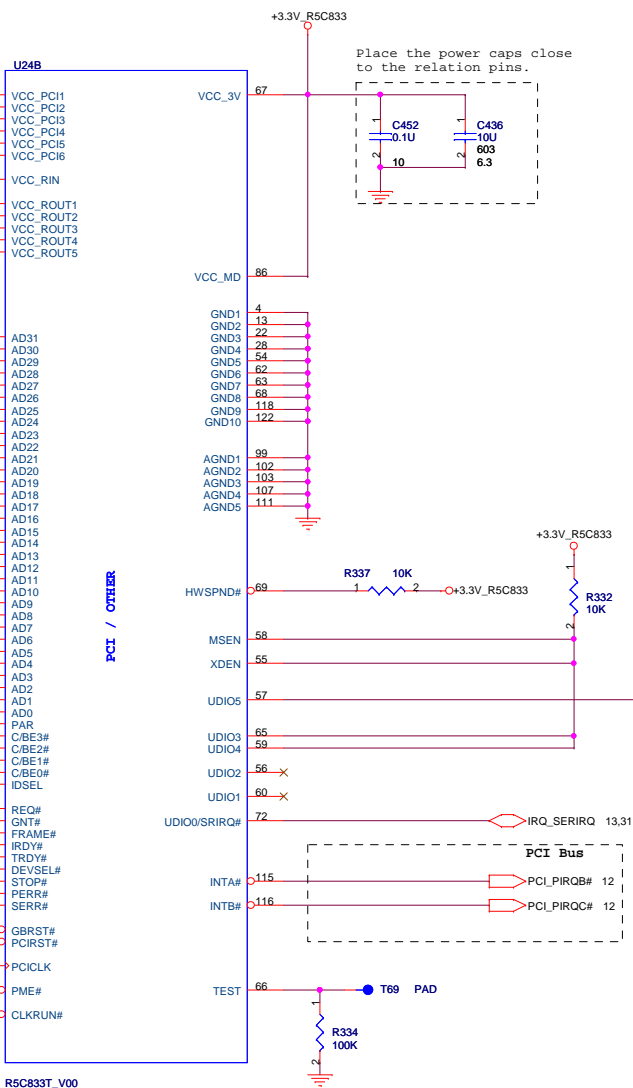
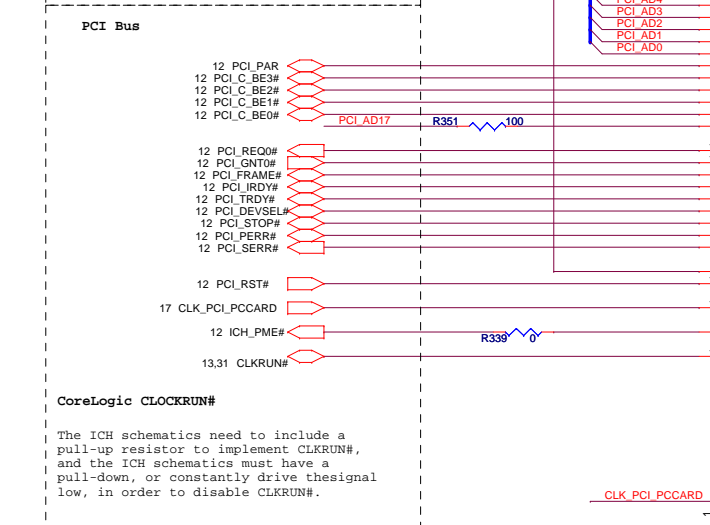
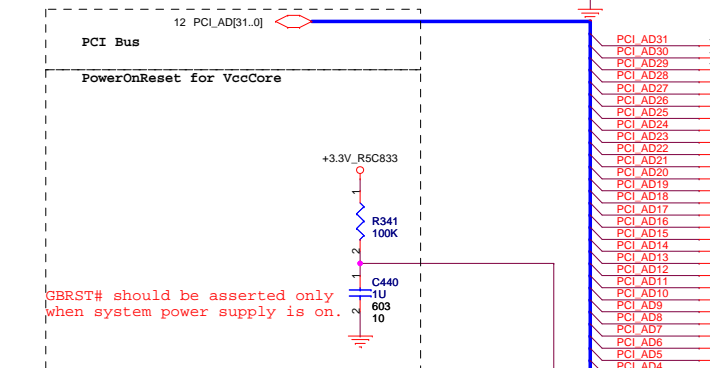
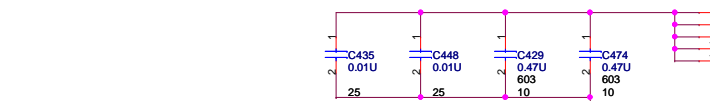
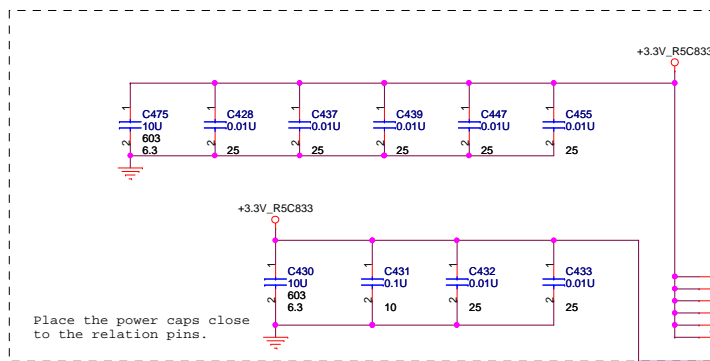
HDMI



| | |
|--|--------|
| | |
| QUANTA COMPUTER | |
| Title LCD CONN & CK-SSCD | |
| Size Document Number FM8 | Rev 2A |
| Date: Friday, November 21, 2008 Sheet 26 of 58 | |



| | | |
|------------------------------------|------------------------|-----------|
| Title CRT&TV CONN | | |
| Size FMS | Document Number FMS | Rev 2A |
| Date: Friday, November 21, 2008 | Sheet 27 | of 58 |



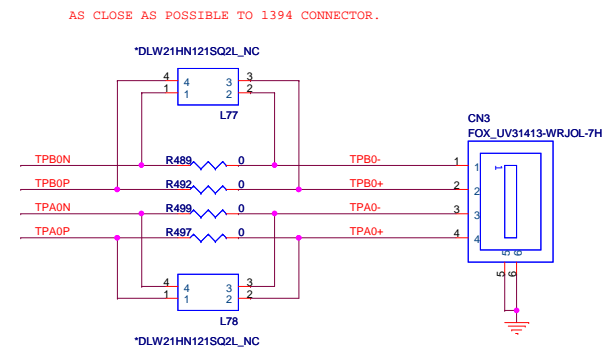
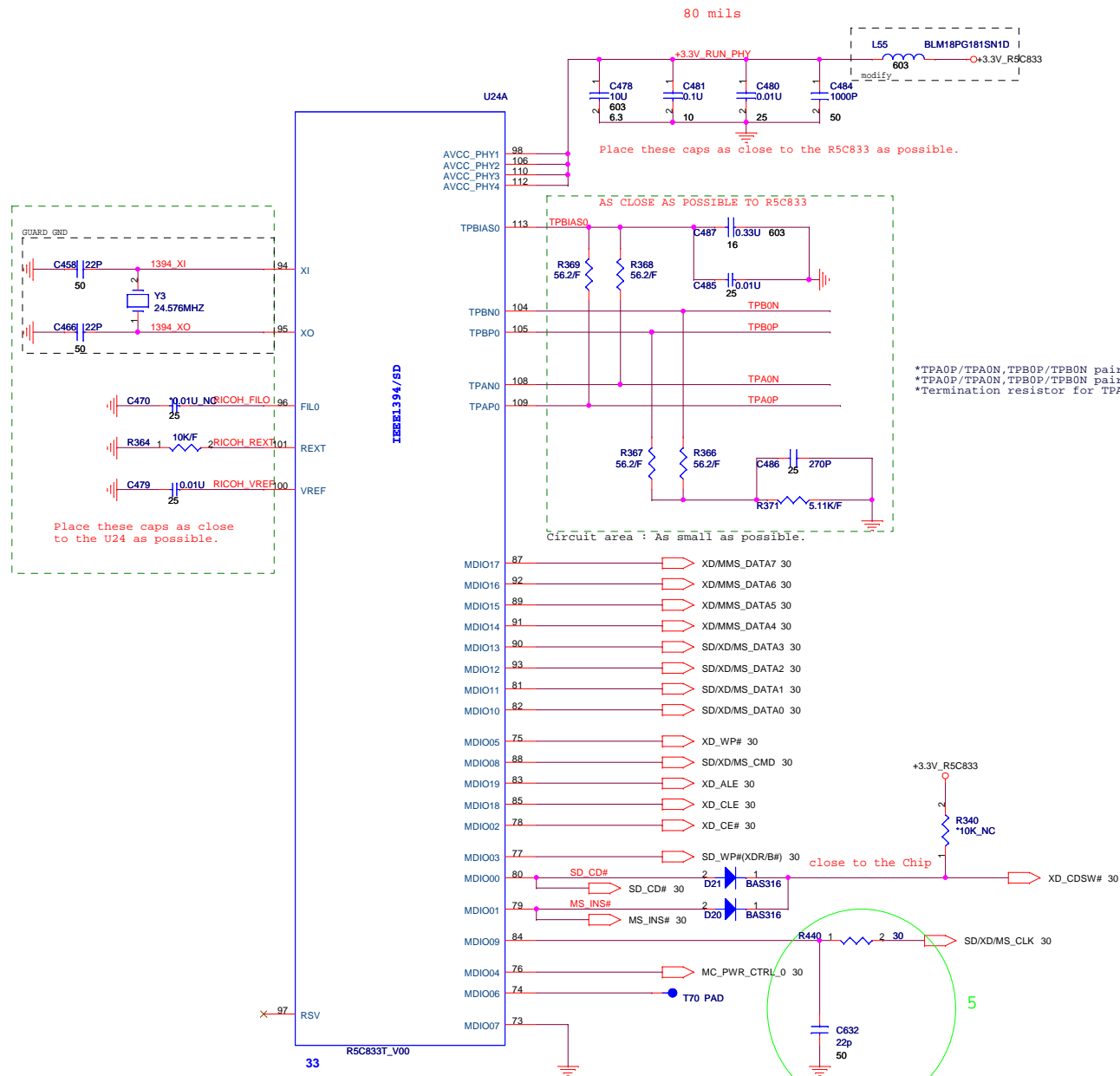
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable

1394 Interrupt
Media card Interrupt

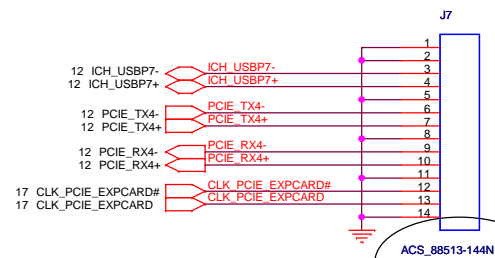
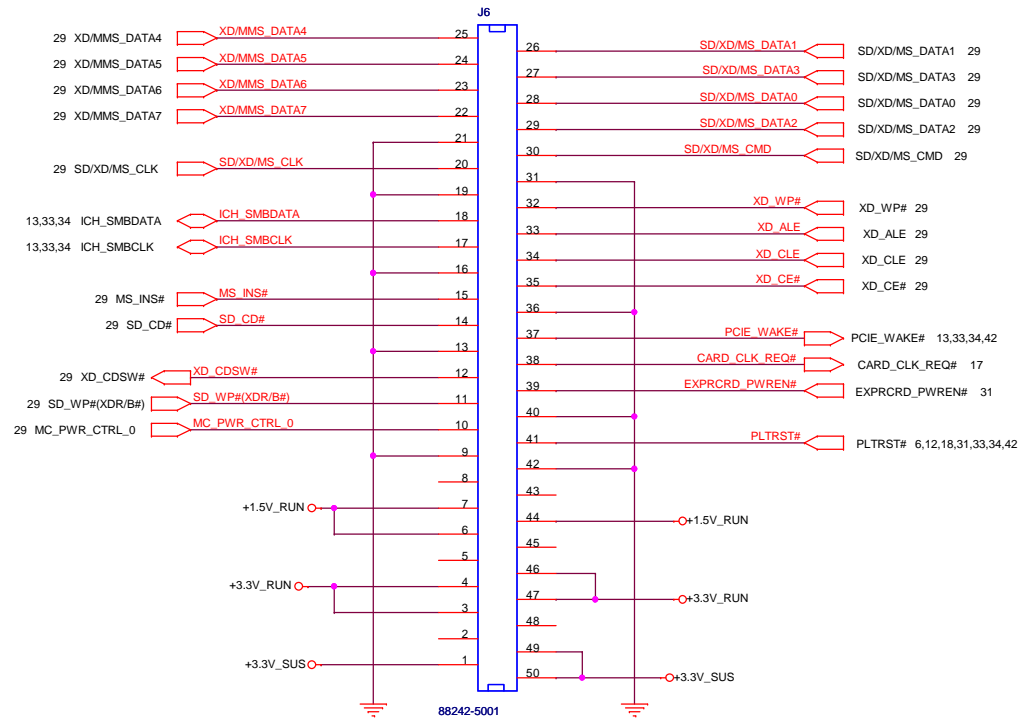


5 IN 1 CONTROLLER

| Size | Document Number | Rev |
|-------|---------------------------|----------------|
| FM8 | | 2A |
| Date: | Friday, November 21, 2008 | Sheet 28 of 58 |

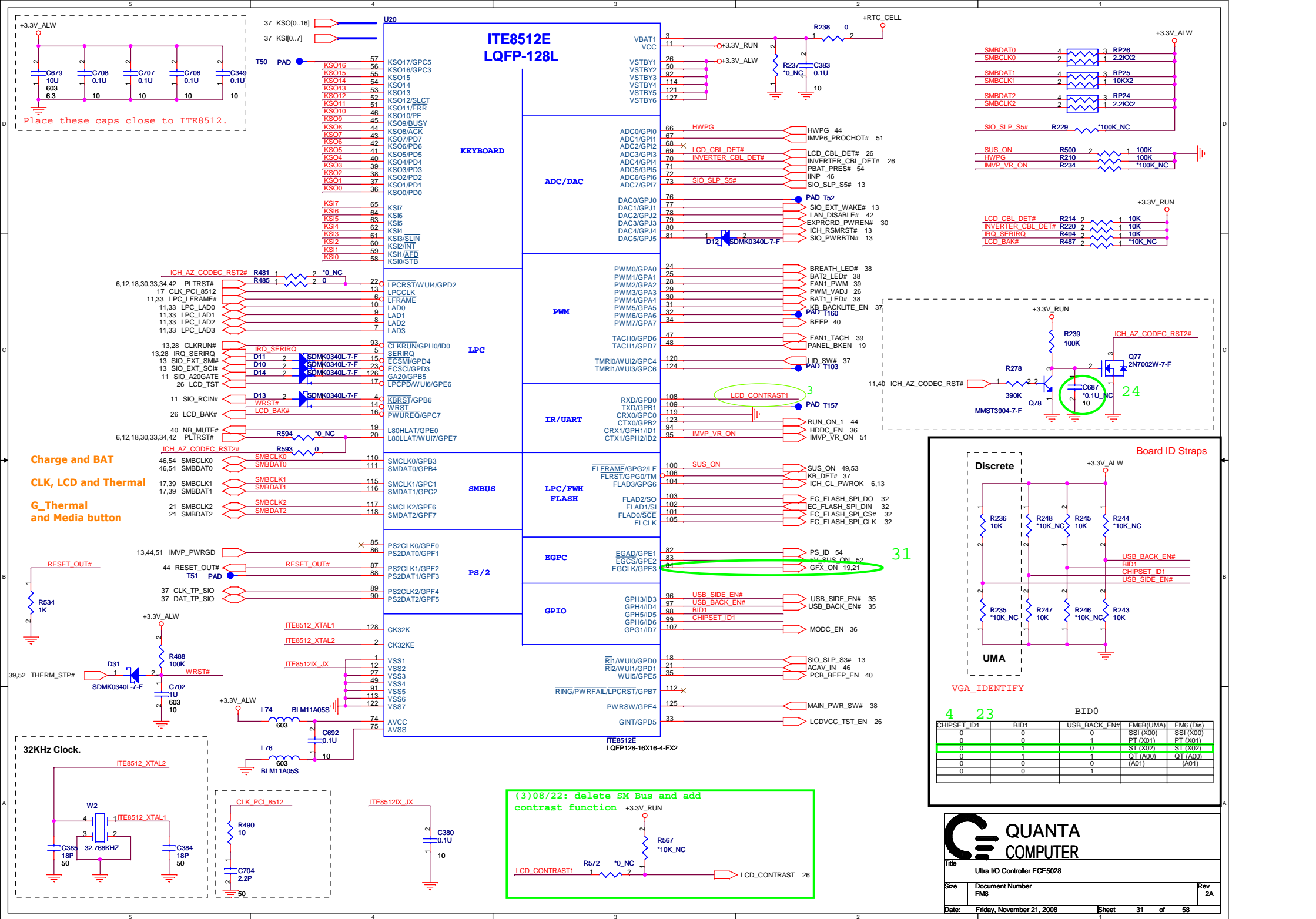


Express Card/CARD READER

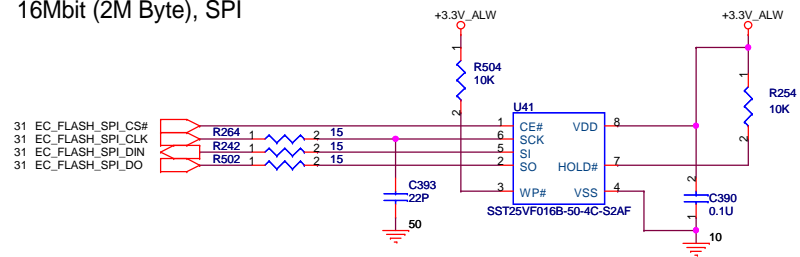


8/28:change PN to 88513-144N

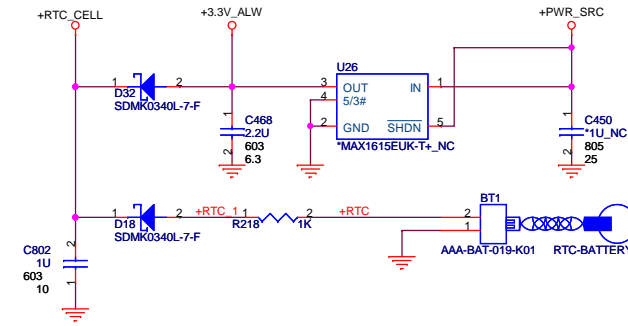
| | | |
|------------------------------|---------------------------|----------------|
| | | |
| QUANTA COMPUTER | | |
| Title: ExpressCard/SmartCard | | |
| Size: | Document Number: FMS | Rev: 2A |
| Date: | Friday, November 21, 2008 | Sheet 30 of 58 |



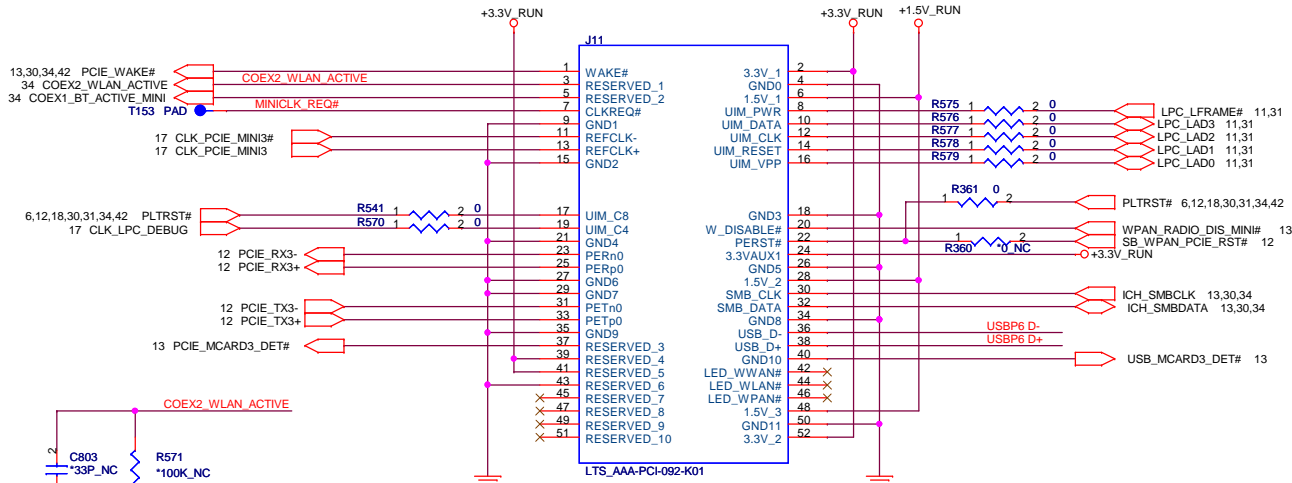
16Mbit (2M Byte), SPI



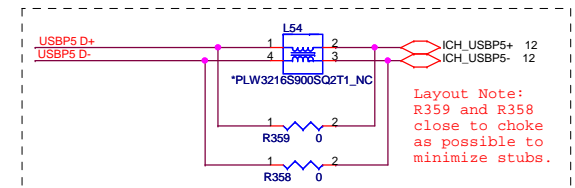
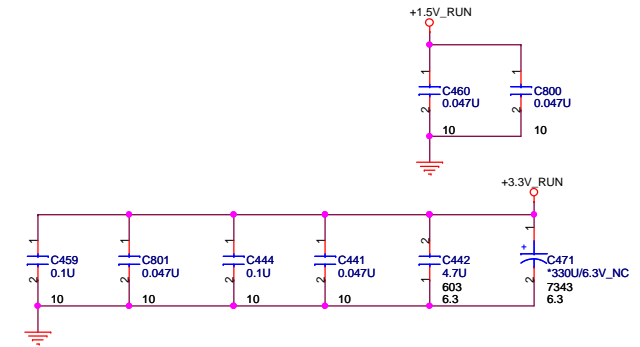
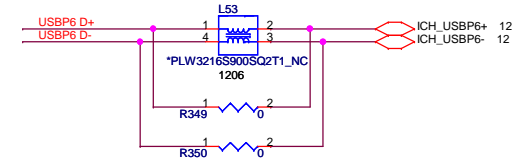
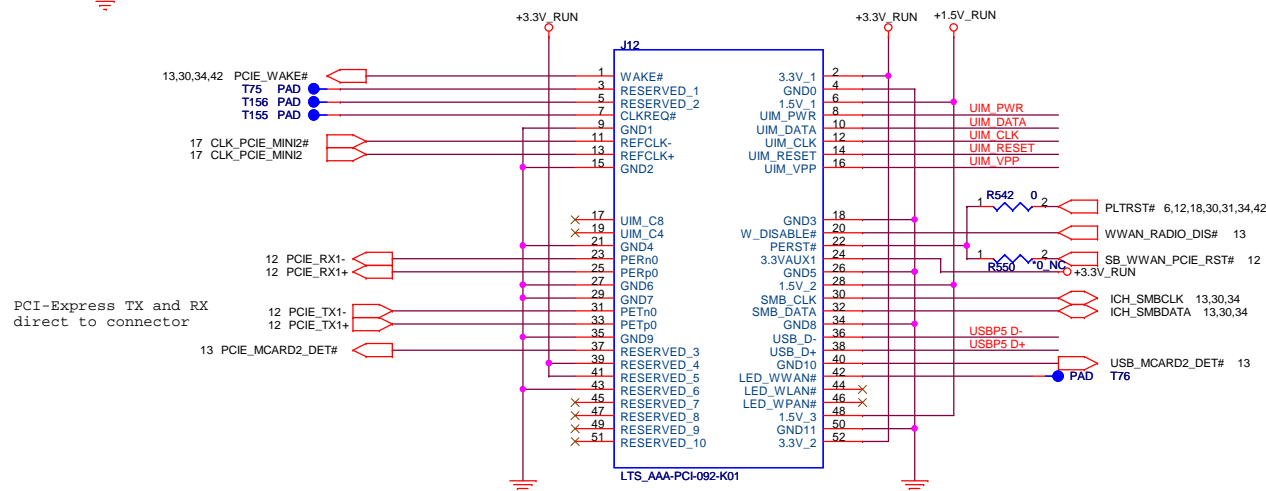
RTC BATTERY



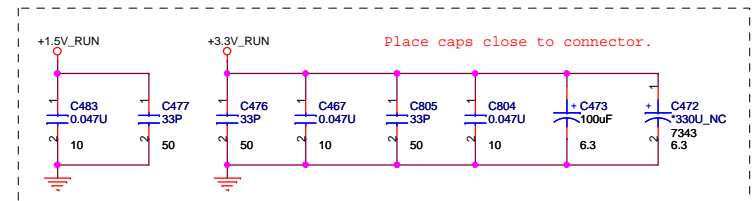
MiniCard Robson, BT. UWB connector



MiniCard WWAN connector



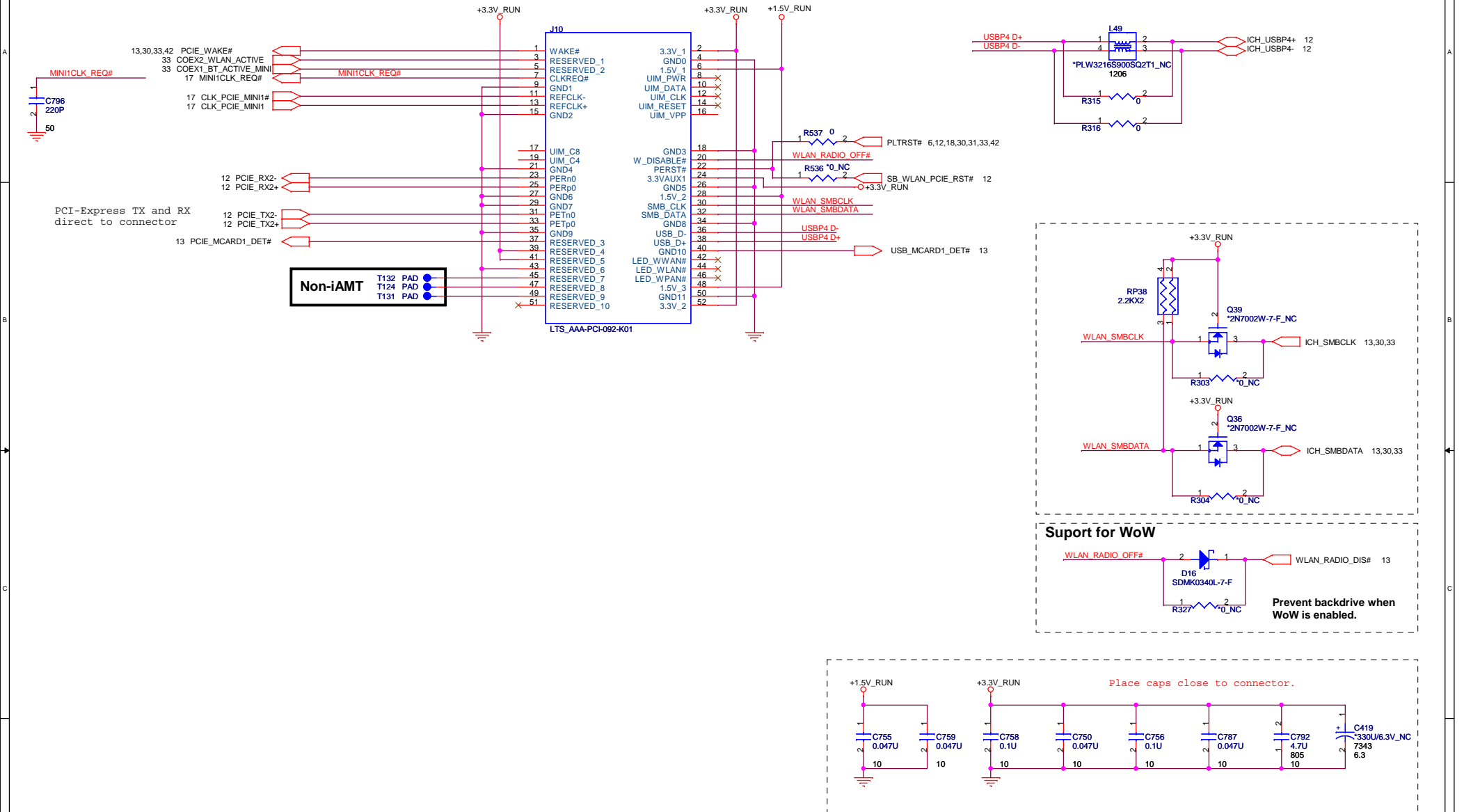
Layout Note:
R359 and R358
close to choke
as possible to
minimize stubs.



| | | | |
|-------|---------------------------|-------|----------|
| Title | | | MINI-PCI |
| Size | Document Number | Rev | |
| FMB | | 2A | |
| Date: | Friday, November 21, 2008 | Sheet | 33 of 58 |

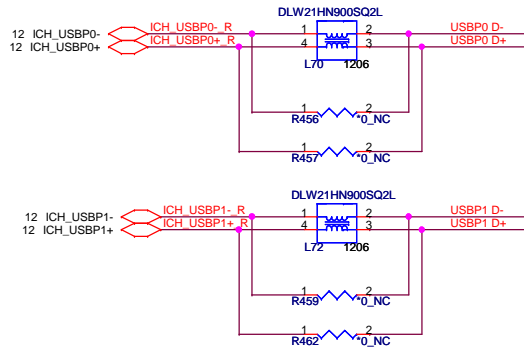
Place as close as possible to JSIM1 connector

MiniCard WLAN connector



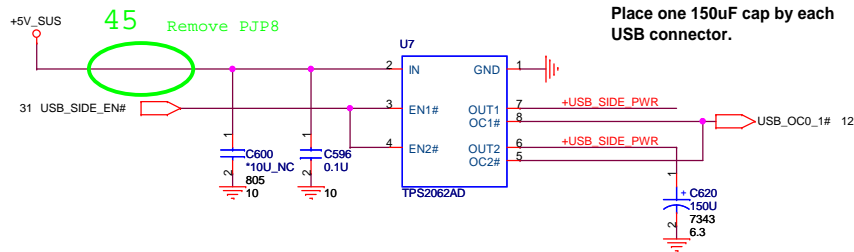
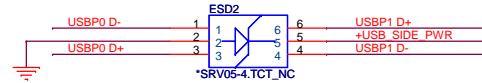
| | | |
|-----------|---------------------------|----------------|
| Title | | |
| MDC CONN. | | |
| Size | Document Number | Rev |
| FM8 | | 2A |
| Date: | Friday, November 21, 2008 | Sheet 34 of 58 |

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

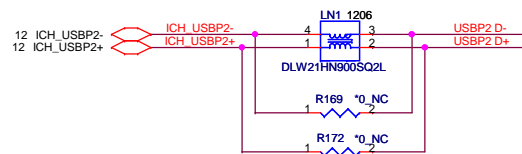


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

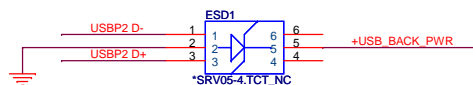
Place ESD diodes as close as USB connector.



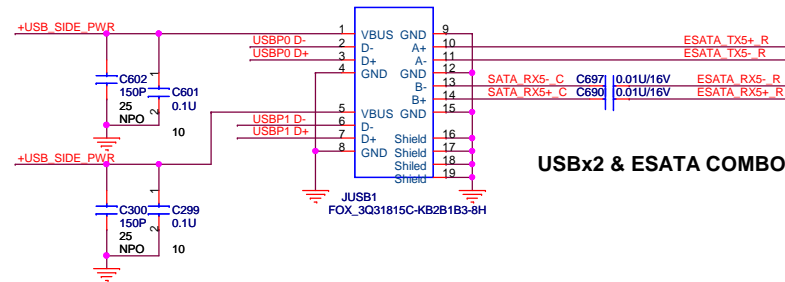
Place one 150uF cap by each USB connector.



Place ESD diodes as close as USB connector.

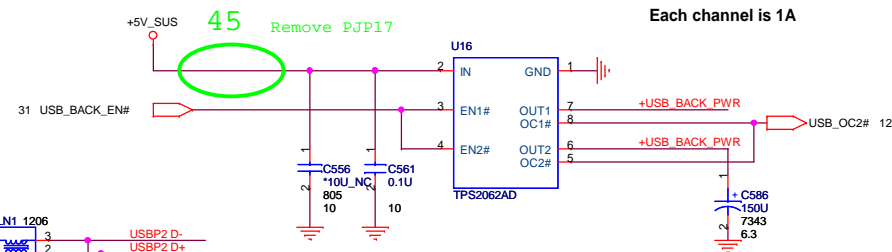
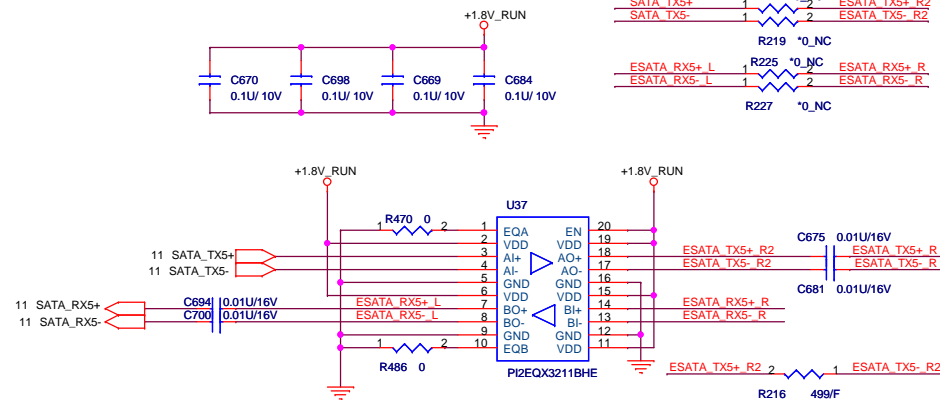


Side External USBX2

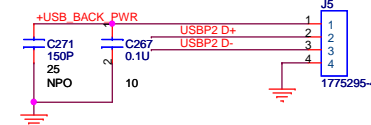


USBx2 & ESATA COMBO

E-SATA Re-driver

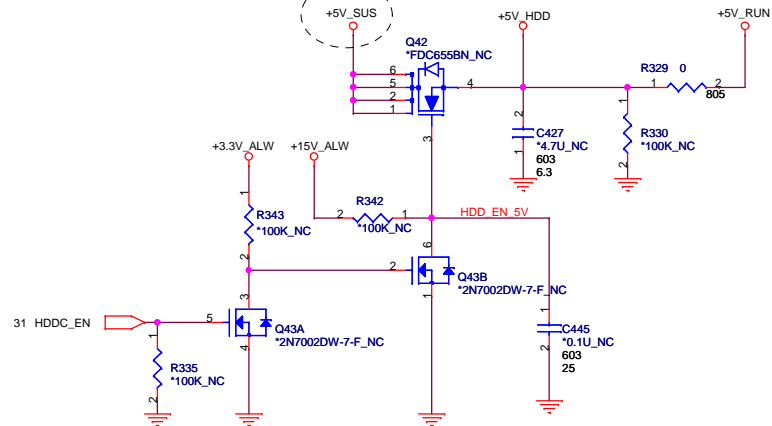
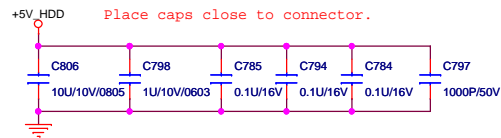
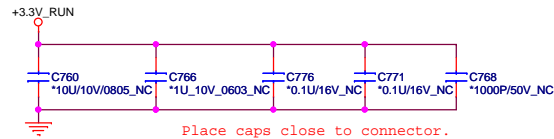
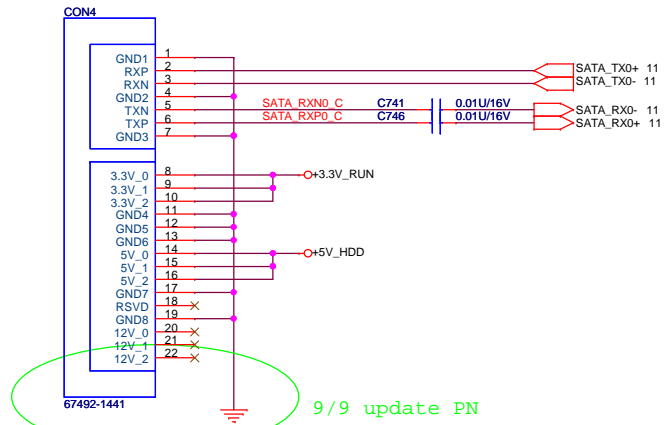


Each channel is 1A

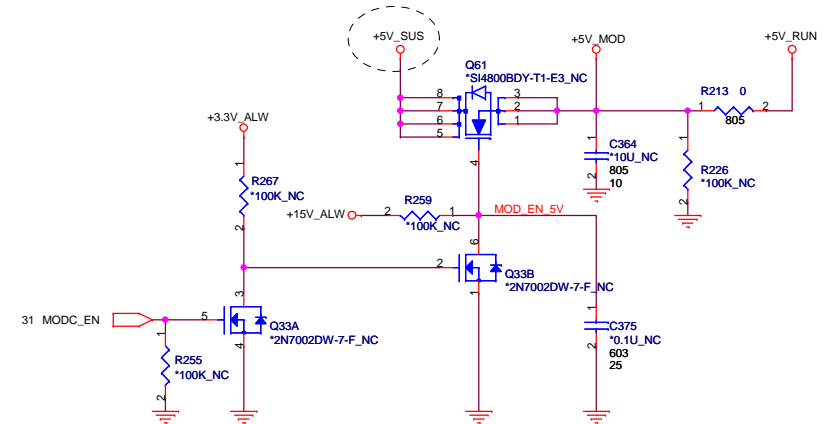
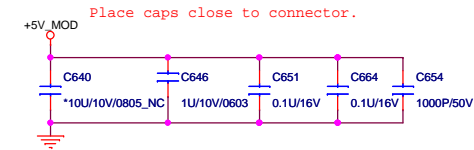
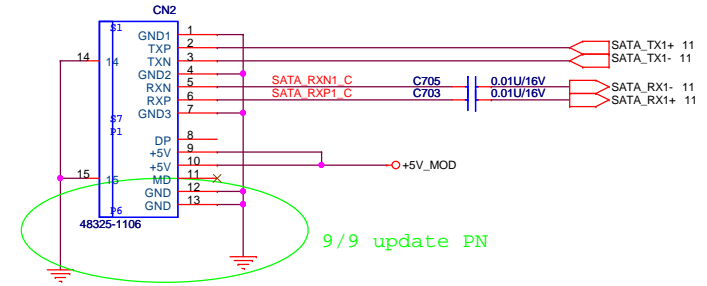


| | | | |
|-------|---------------------------|-------|-------------------|
| Title | | | SERIAL PORT & USB |
| Size | Document Number | Rev | |
| | FM8 | 2A | |
| Date: | Friday, November 21, 2008 | Sheet | 35 of 58 |

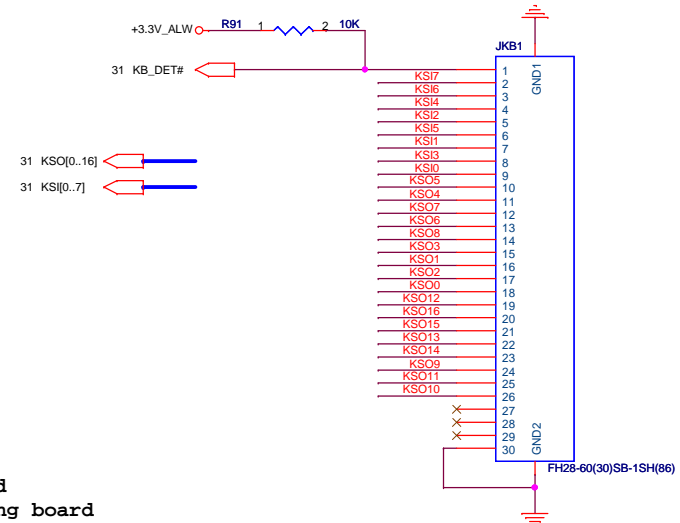
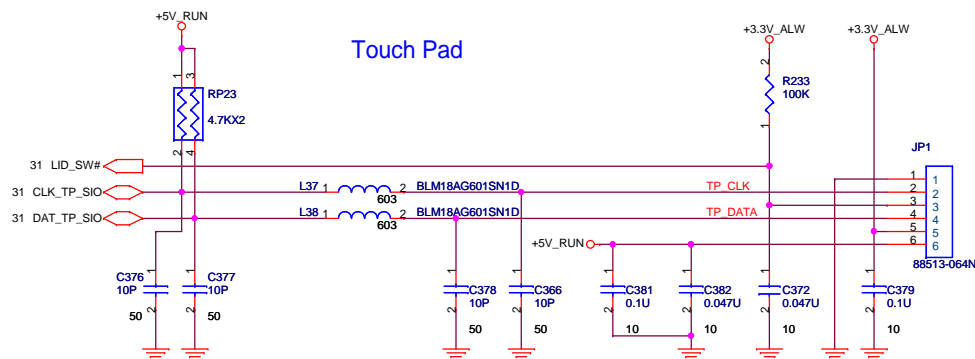
SATA Connector.



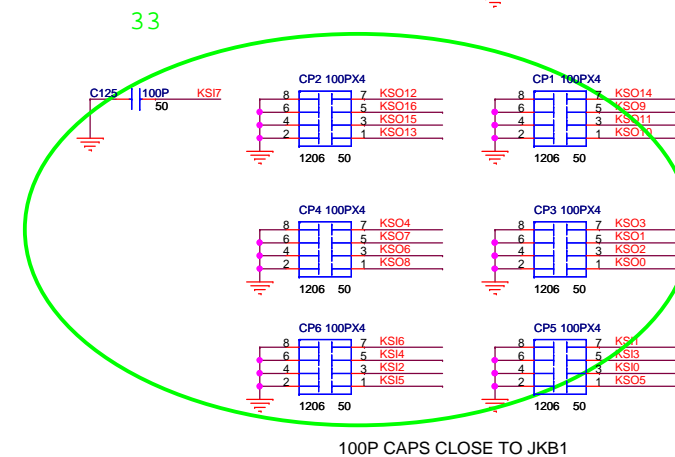
ODD Connector



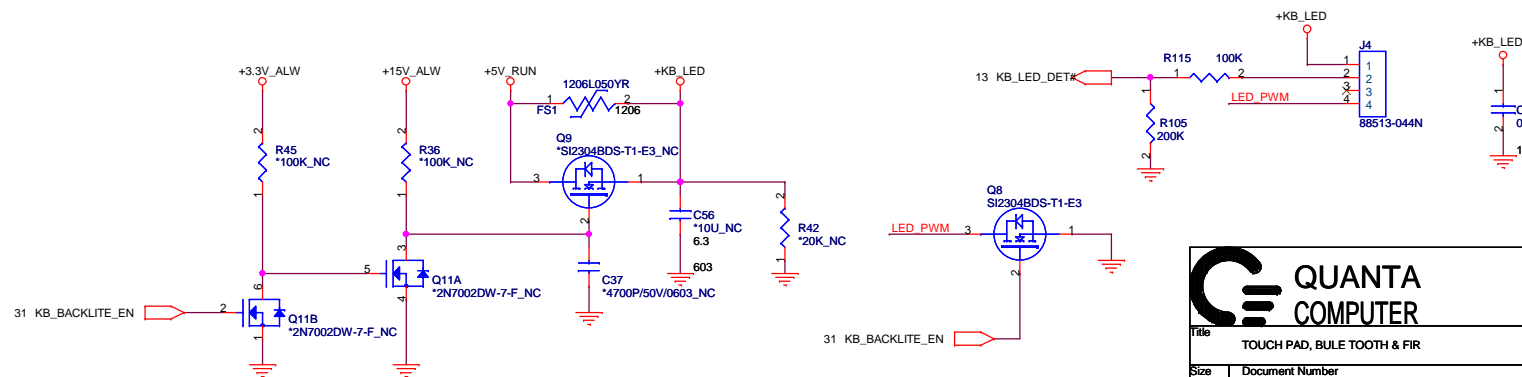
| | | | |
|-------|---------------------------|-------|-------------------|
| Title | | | SATA (HDD&CD_ROM) |
| Size | Document Number | Rev | |
| | FMB | 2A | |
| Date: | Friday, November 21, 2008 | Sheet | 36 of 58 |



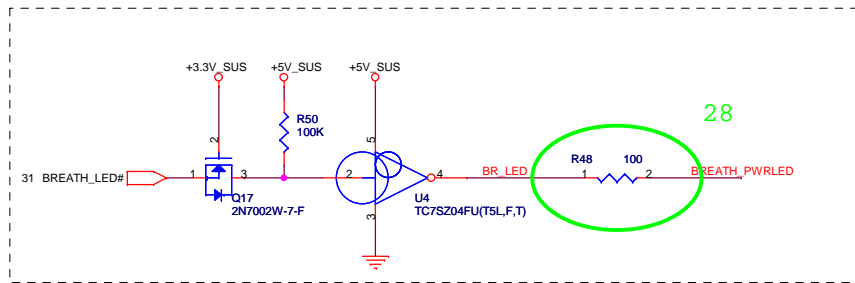
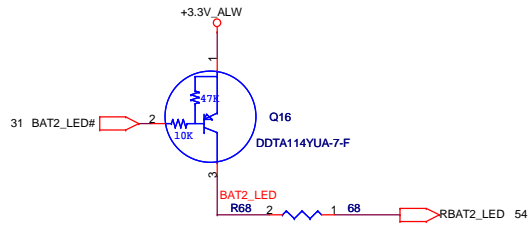
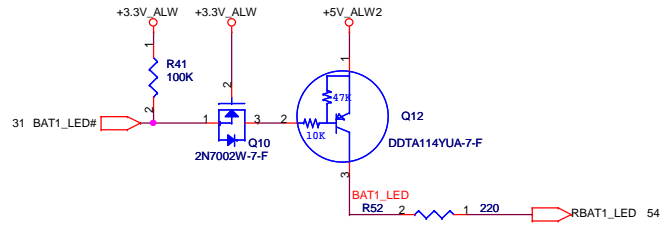
08-05 add
For running board



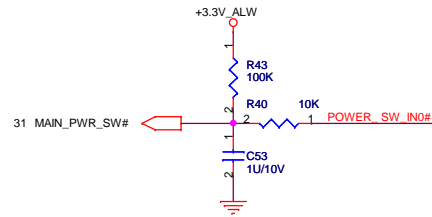
Key board Illumination



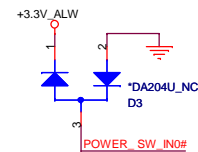
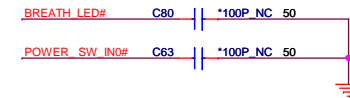
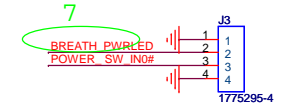
Battery status.

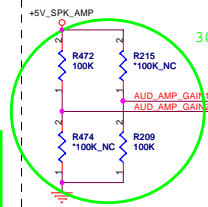
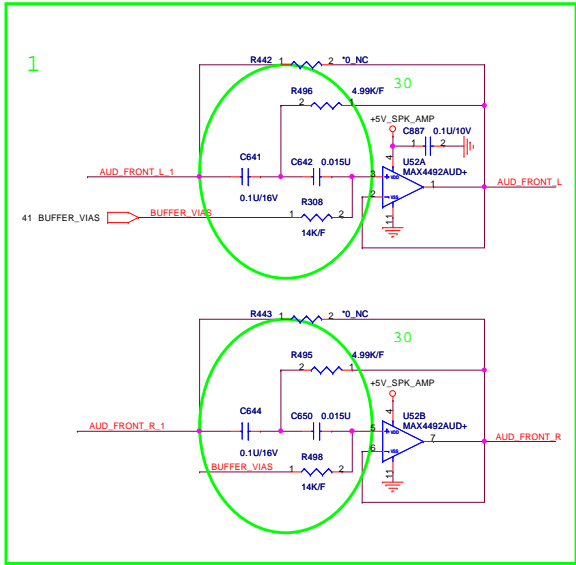


Power Switch

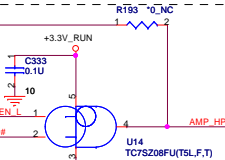
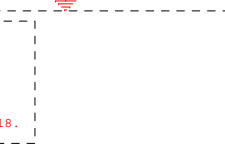
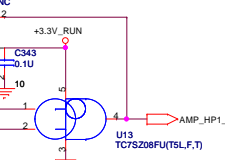
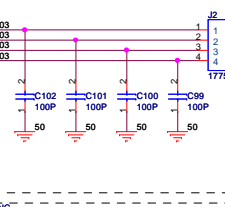
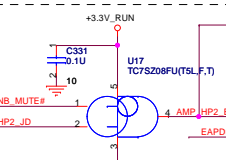
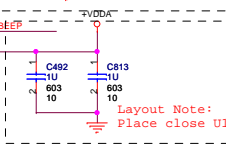
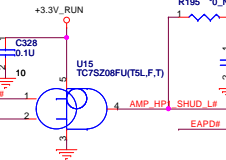
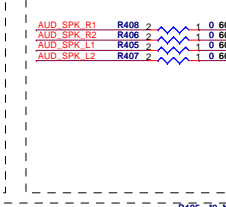
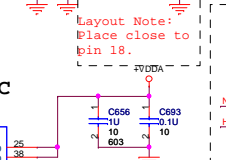
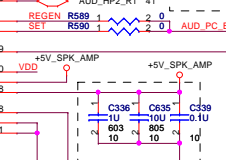
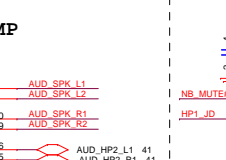
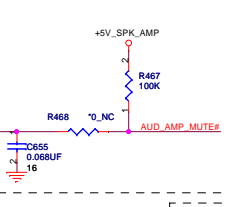
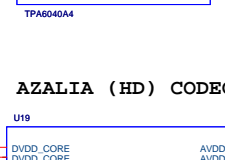
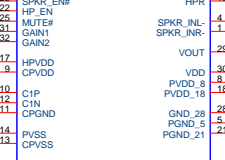
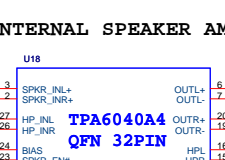
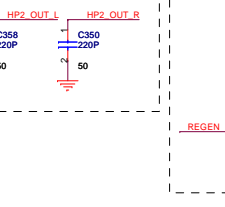
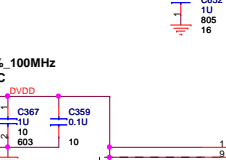
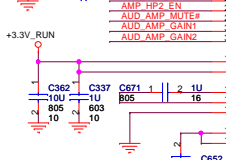
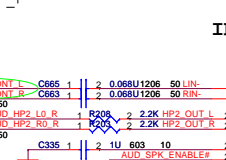
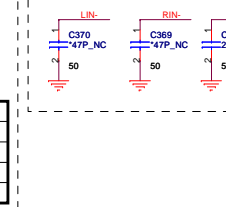
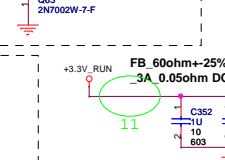
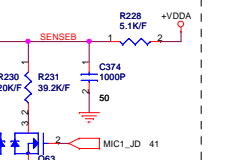
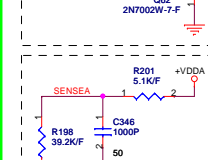
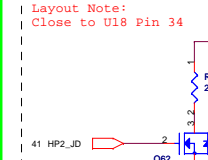
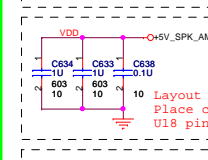


Power button cable

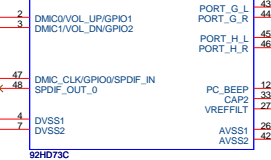
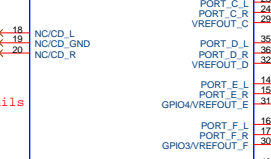
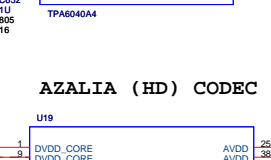
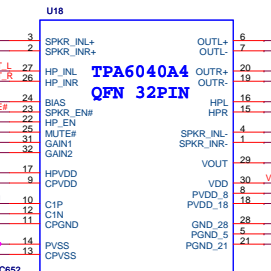




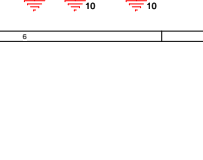
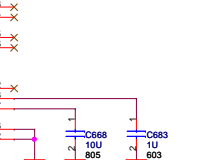
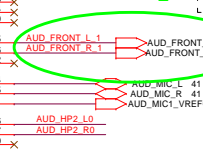
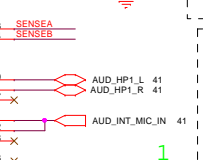
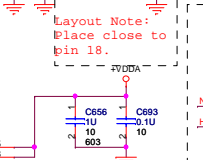
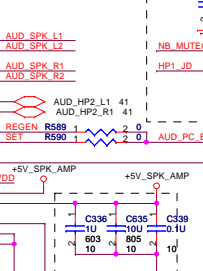
| GAIN1 | GAIN2 | GAIN |
|-------|-------|--------|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |



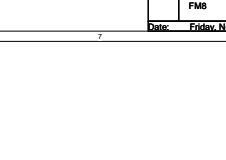
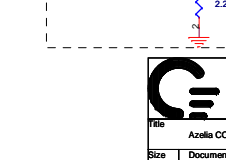
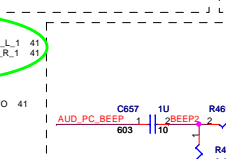
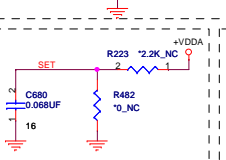
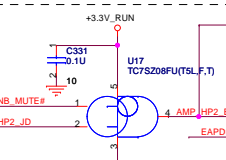
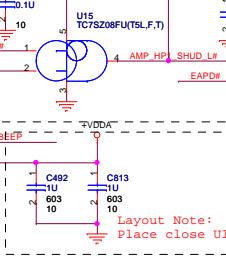
INTERNAL SPEAKER AMP



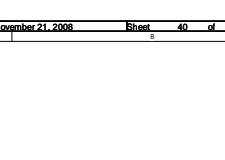
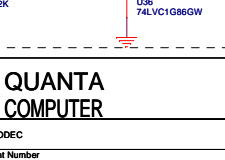
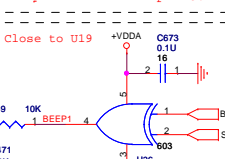
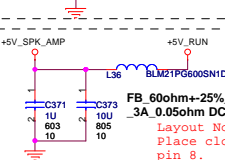
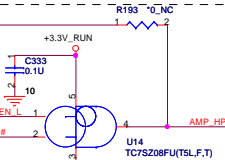
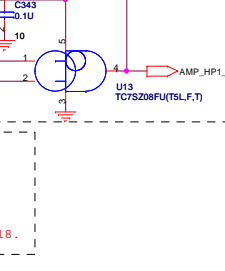
AZALIA (HD) CODEC



INTERNAL SPEAKER AMP

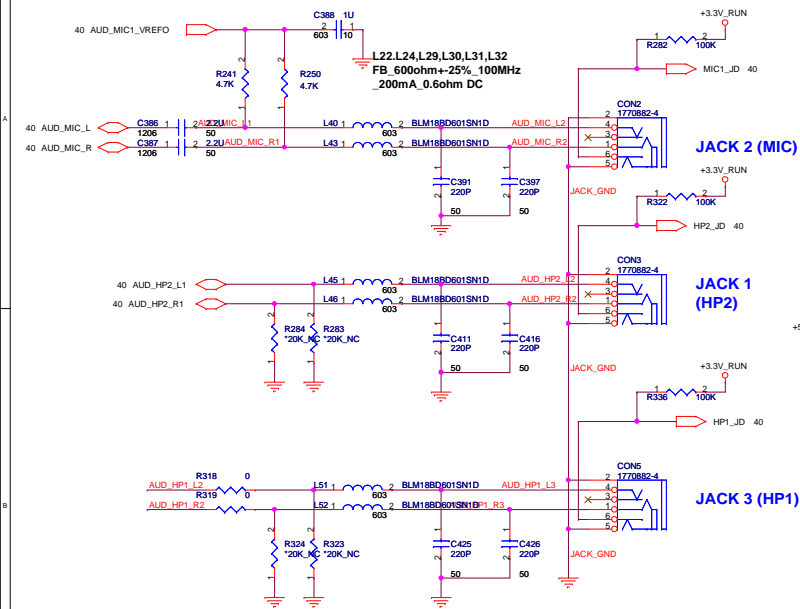


AZALIA (HD) CODEC

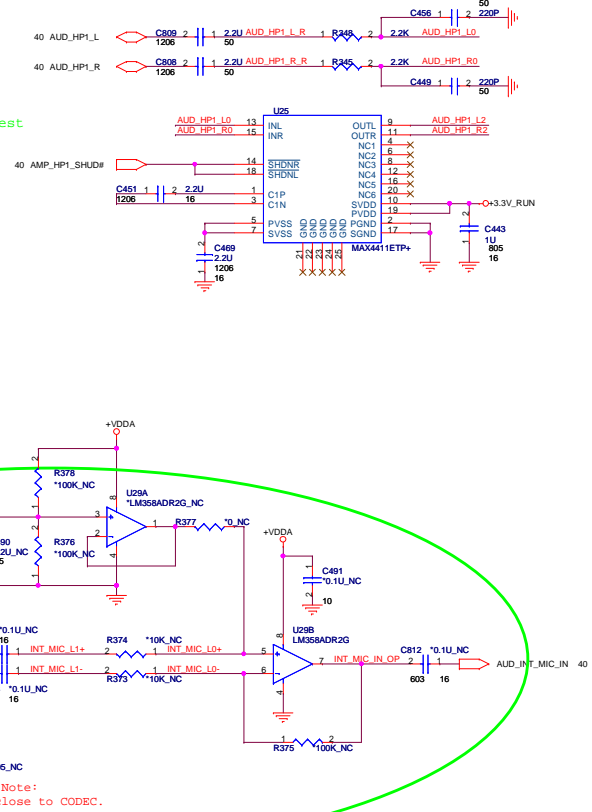
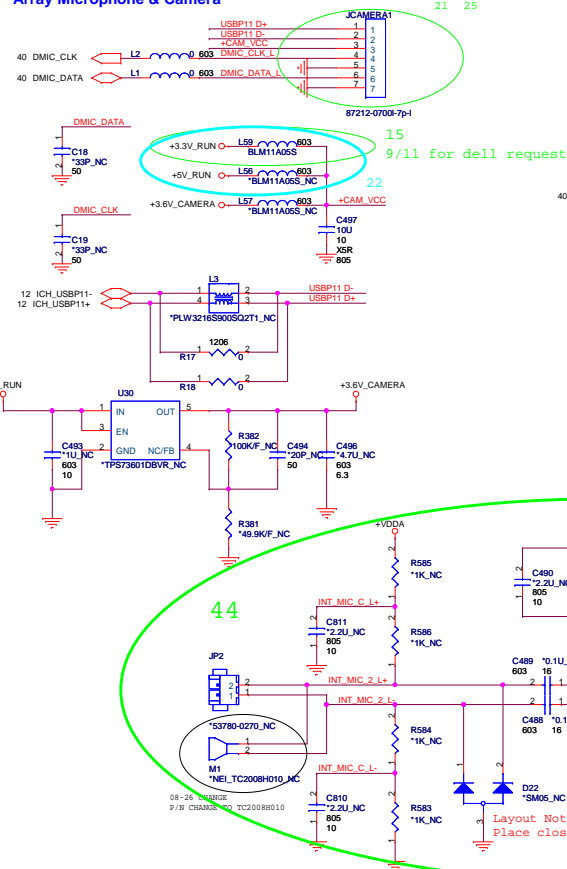


file
Azalia CODEC
Size
Document Number
PMB
Date
Friday, November 21, 2008
Sheet
40 of 58
Rev
2A

Headphone Jack
Stereo MIC Jack

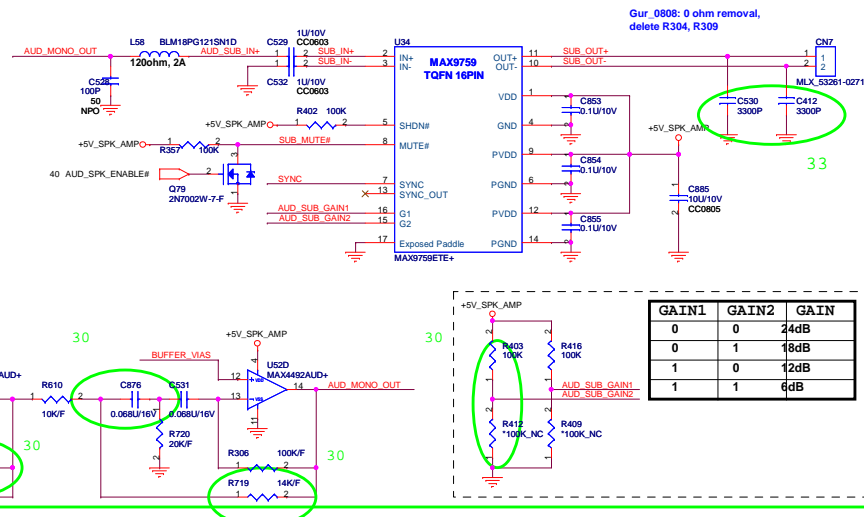


Array Microphone & Camera

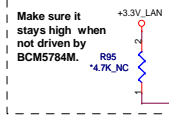
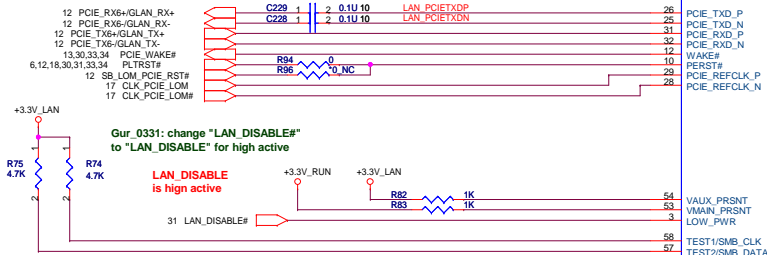
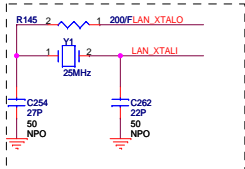
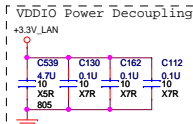
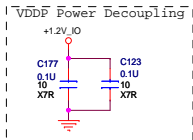
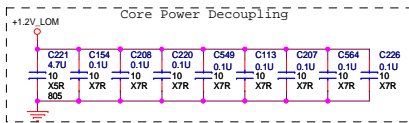


INTERNAL SUBWOOFER AMP

| SYNC | Condition |
|---------|--|
| VDD | Spread-spectrum mode with fS = 1200kHz \pm 70kHz. |
| GND | Fixed-frequency mode with fS = 1100kHz. |
| FLOAT | Fixed-frequency mode with fS = 1500kHz. |
| Clocked | Fixed-frequency mode with fS = external clock frequency. |



| GAIN1 | GAIN2 | GAIN |
|-------|-------|------|
| 0 | 0 | 24dB |
| 0 | 1 | 18dB |
| 1 | 0 | 12dB |
| 1 | 1 | 6dB |



BCM5784M
10mm x 10mm
68-Pin QFN

Note: thermal pad

U9

DCVDDP

BIASVDDH

XTALVDDH

AVDDU/AVDDH

DC/AVDDH

DC/AVDDH

TRD3_N

TRD3_P

AVDDH/TRD2_N

TRD2_N/TRD2_P

TRD2_P/AVDDH

AVDDH/TRD1_N

TRD1_N/TRD1_P

TRD1_P/AVDDH

TRD0_N

TRD0_P

LINKLED

SPD100LED

SPD100LED

TRAFFICLED

GPIQ2

UART_MODE

GPIQ1_SERIALD

GPIQ0_SERIALD

SClk_EECLK

SO_EEDATA

ENERGY_DET

VDDC_IOVDDP

REGOUT12_IO/REGCTL25

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

REGCTL12

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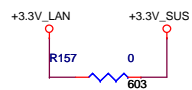
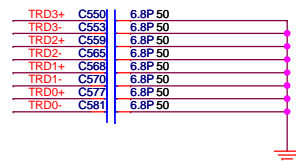
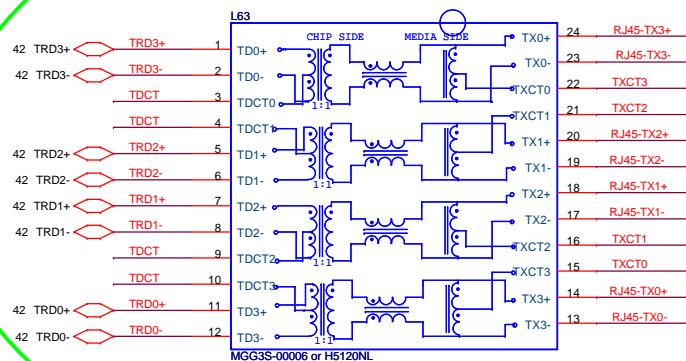
Remove LAN LED function

R78 & R76: Stuff only if U5 is installed

39

50

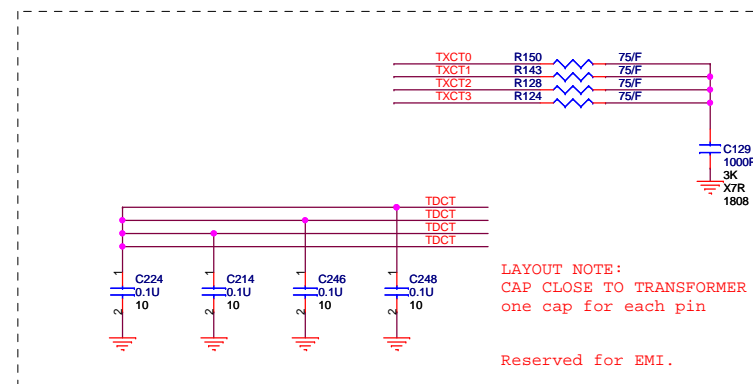
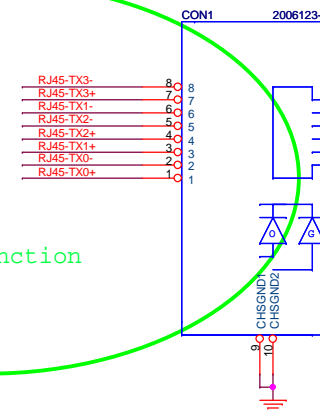
TRANSFORM

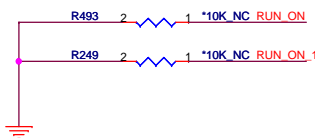
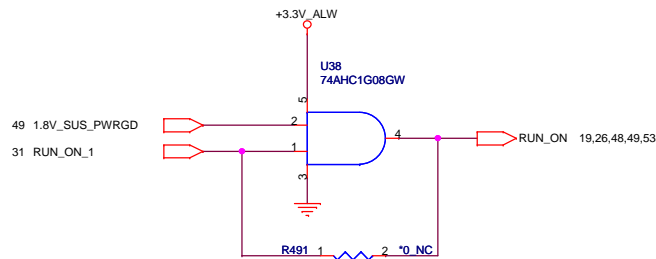
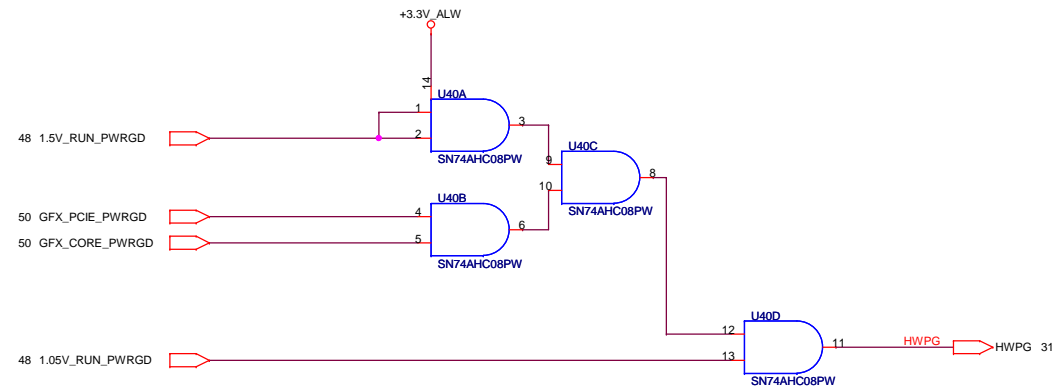
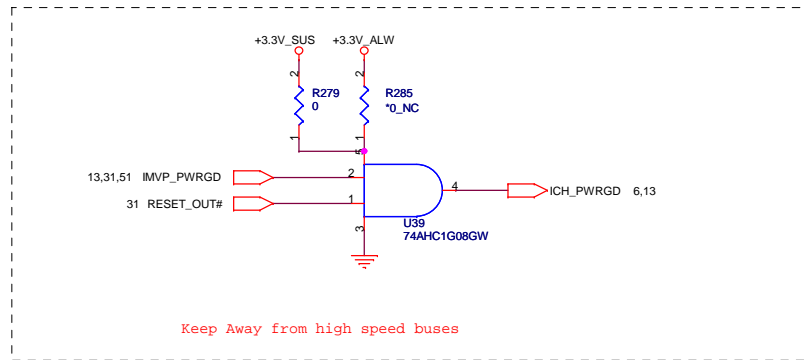


RJ-45 Connector


27

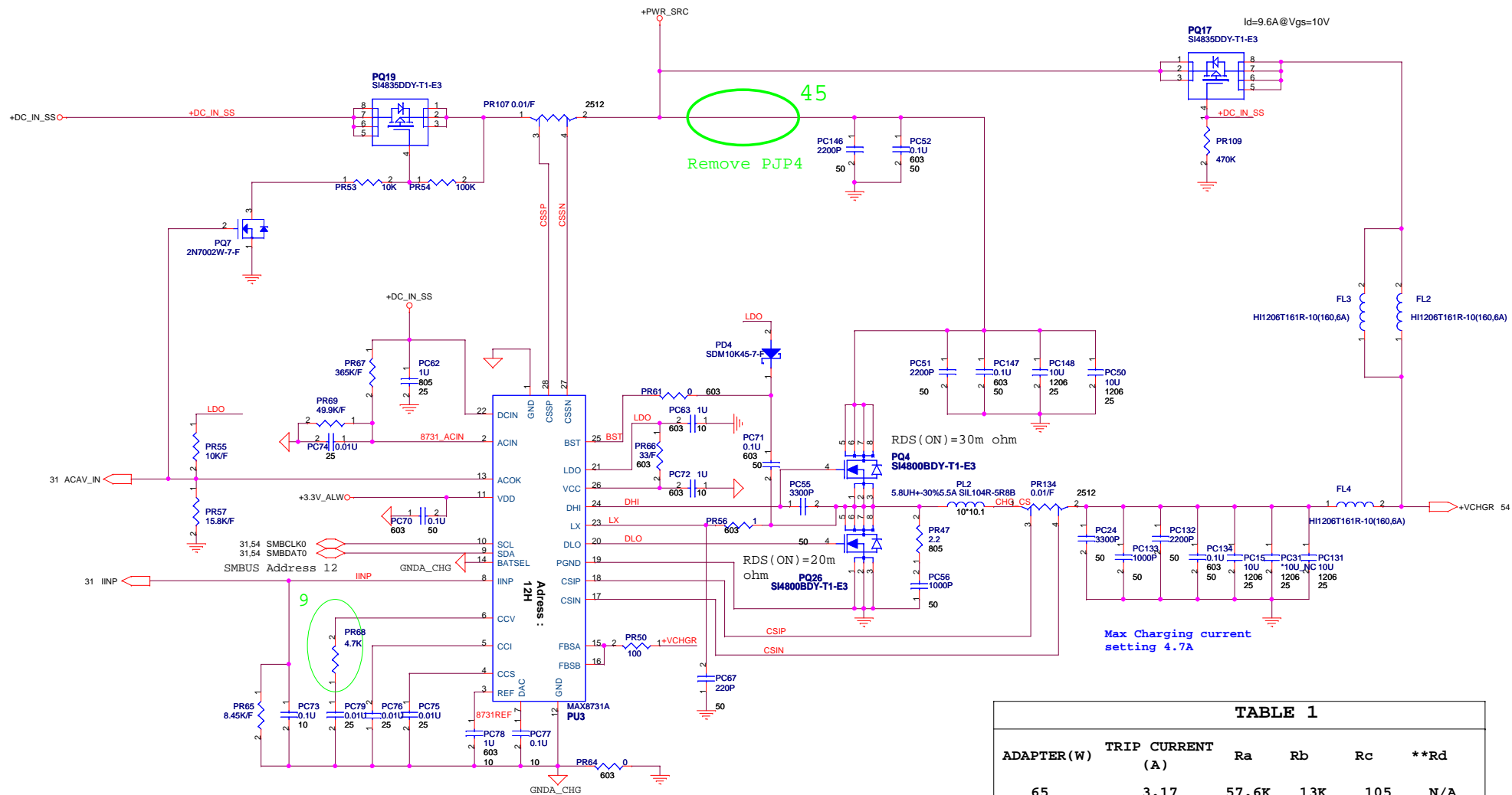
Remove LAN LED function





| | | | | | |
|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 |
| A | | | | | |
| B | | | | | |
| C | | | | | |
| D | | | | | |

| | | |
|--|------------------------|-----------|
|  QUANTA COMPUTER | | |
| Title Battery Selector | | |
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| ADAPTER (W) | TRIP CURRENT (A) | Ra | Rb | Rc | **Rd |
|-------------|------------------|-------|-------|-----|-------|
| 65 | 3.17 | 57.6K | 13K | 105 | N/A |
| 90 | 4.43 | 51.1K | 17.8K | 348 | 33.2K |
| 130 | 6.43 | 32.4K | 20.5K | 100 | 27.4K |
| 150 | 7.43 | 30.9K | 24.9K | 432 | 88.7K |
| 200 | 9.75 | 19.1K | 28K | 301 | 36.5K |
| 230 | (see note3) | 32.4K | 6.49K | 115 | N/A |


Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.

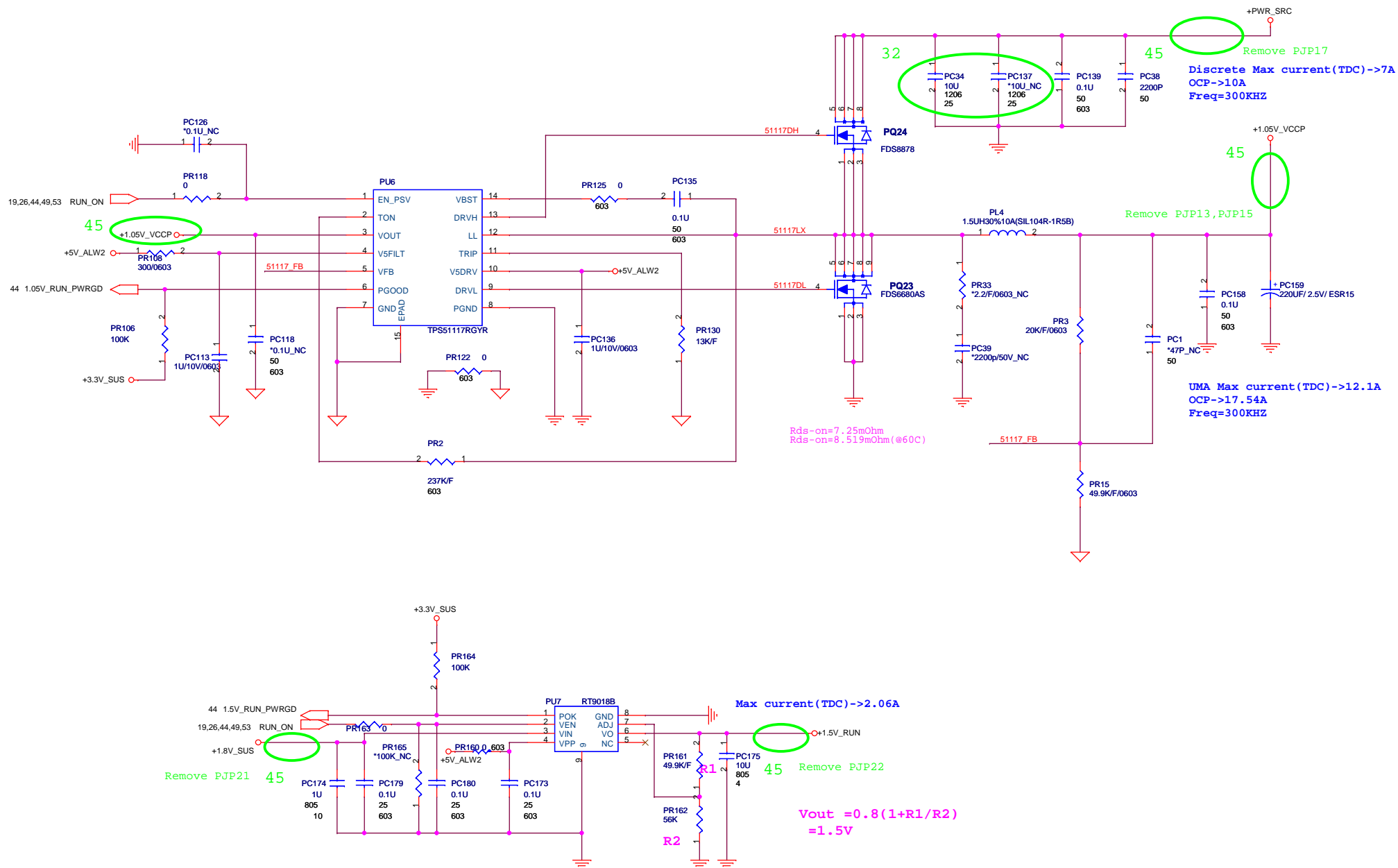
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

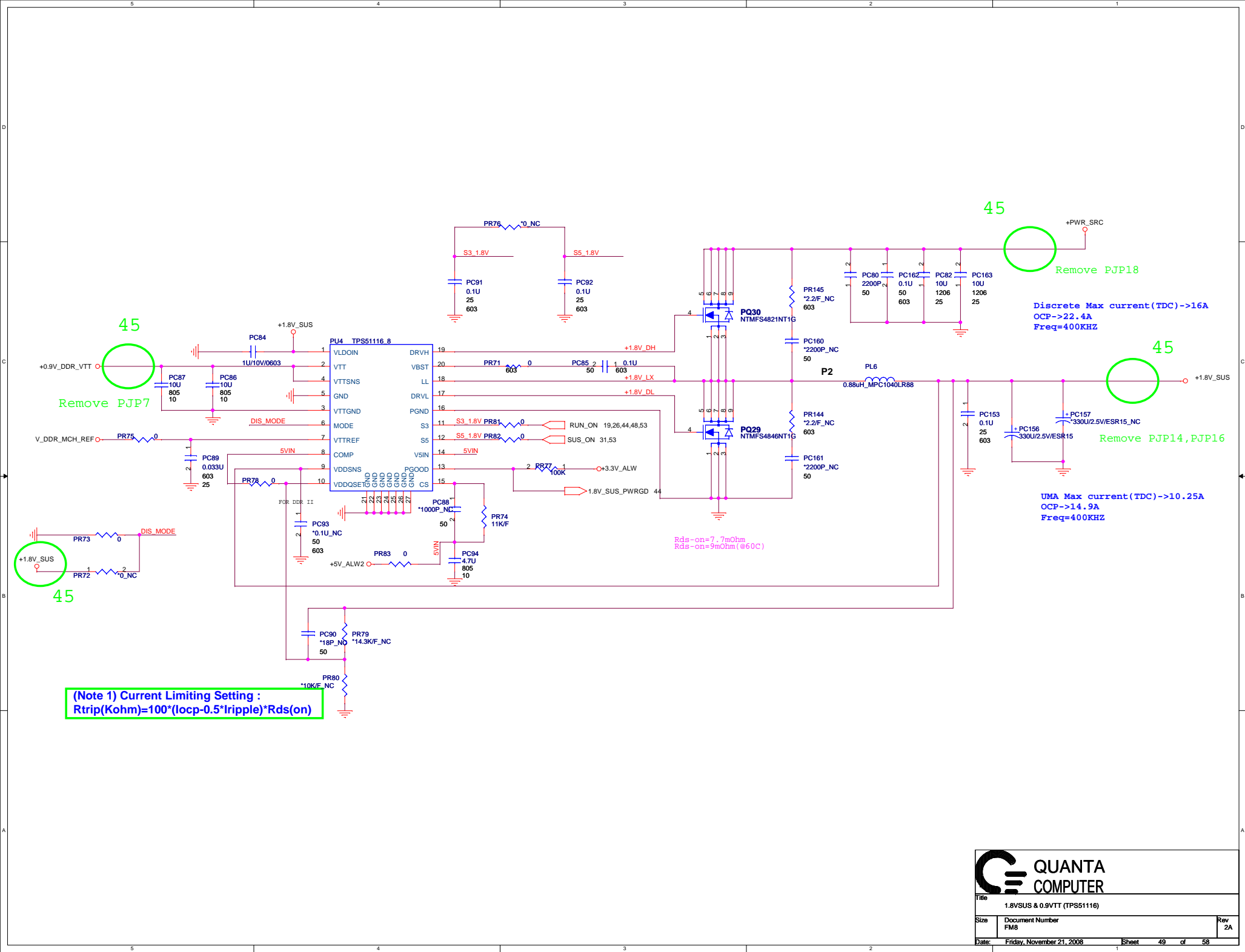
Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

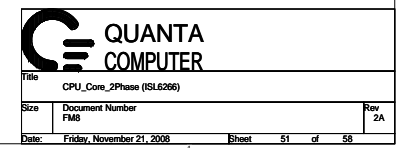
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

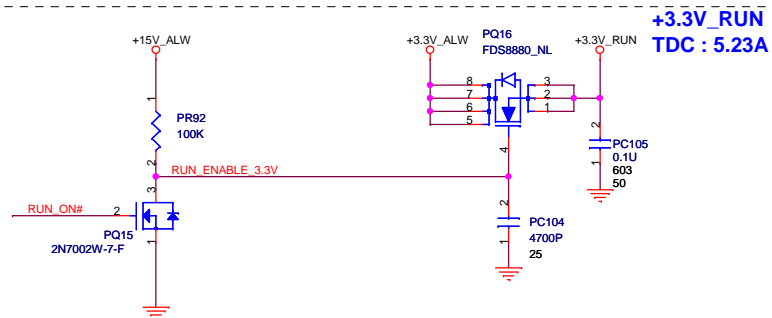
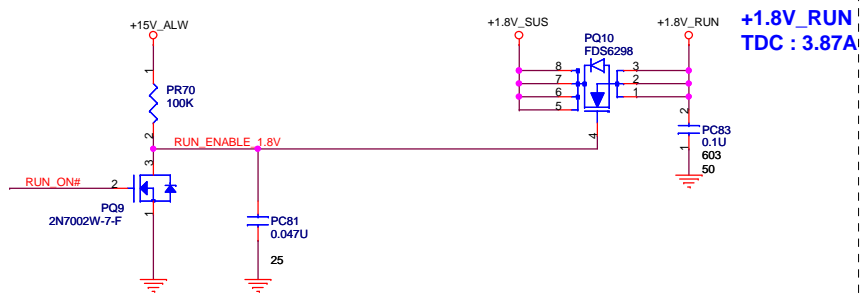
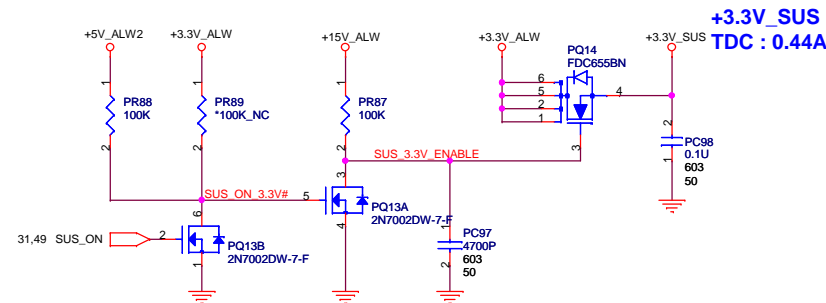
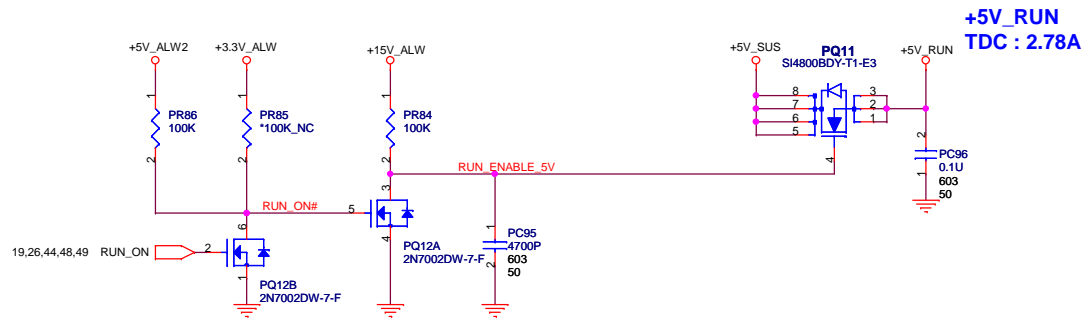
| | | |
|--|--------------------------------|--|
|  QUANTA COMPUTER | | |
| <small>Title</small> | | |
| <small>Size</small> | <small>Document Number</small> | <small>Rev</small> |
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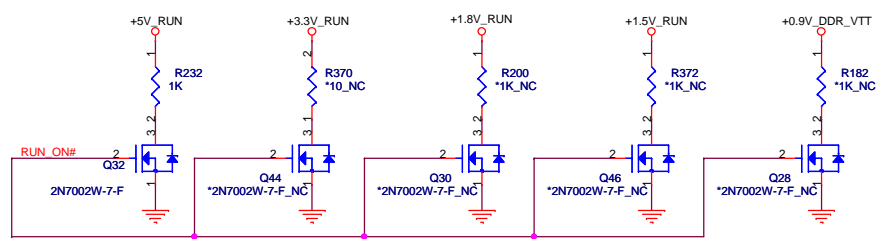


(Note 1) Current Limiting Setting :
 $R_{trip}(Kohm)=100 \times (I_{ocp}-0.5 \times I_{ripple}) \times R_{ds(on)}$

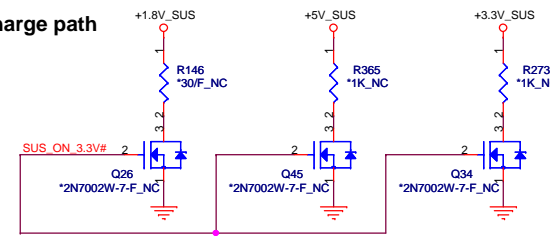




Reserve discharge path

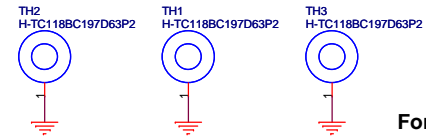
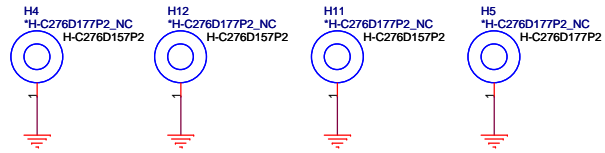


Reserve discharge path

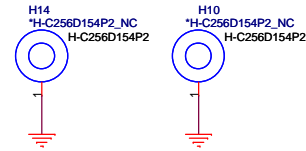
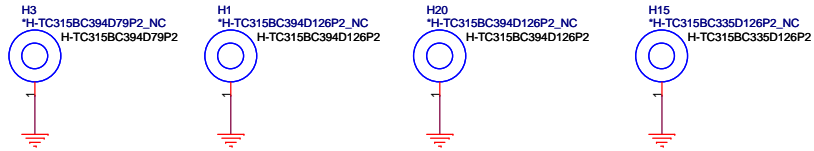


| | | | |
|-------|---------------------------|-------|--------------|
| Title | | | RUN POWER SW |
| Size | Document Number | Rev | |
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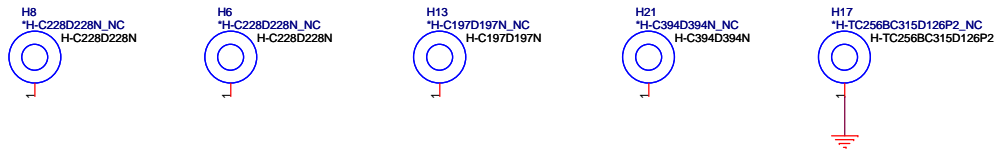
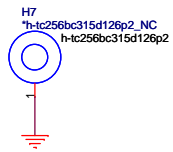
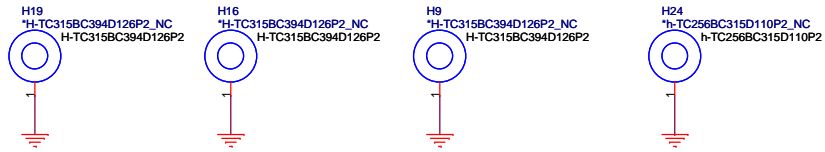
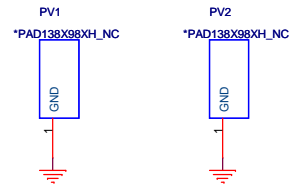
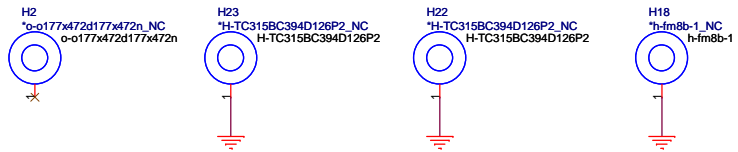
FOR CPU use



For MiniCard nut use.
on 31' header




For GPU nut use.



| | | |
|------------------------------------|------------------------|-----------|
| Title SCREW PAD | | |
| Size FM8 | Document Number FM8 | Rev 2A |
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Reserved for EMI.



QUANTA
COMPUTER

| | | |
|---------|---------------------------|----------------|
| Title | | |
| EMI CAP | | |
| Size | Document Number | Rev |
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